KEEN SIDE electronics

DATASHEET

TFT MODULE

MODULE NO. :

KSET02406N-A40

Customer:
Approved by:

Approved by	Checked by	Prepared by

RECORDS OF REVISION

Part Number	Revision	Revision Content	Revised on
KSET02406N-A40	1.0	First issue	Nov. 19th, 2021

CONTENTS

1. General Specifications

Feature		Spec
Display Spec	Size	2.4 inch
	Resolution	320(RGB) x 240
	Interface	MCU
	Technology type	a-si TFT
	Pixel pitch(mm)	0.153 x 0.153
	Display colors	TN
	TFT Driver IC:	ILI9341
	Viewing Direction	12:00
Mechanical Characteristics	LCM(W x H x D)(mm)	60.26 x 42.72x 2.30
	Active Area(mm)	36.72 x 48.91
	Weight (g)	TBD
	LED Numbers	4 LEDS

Note 1: Viewing direction for best image quality is different from TFT definition; there is a 180 degree shift.
Note 2: Requirements on Environmental Protection: RoHS.
Note 3: LCM weight tolerance: +/-5%.

2. Input/Output Terminals

<table>
<tr><th>No.</th><th>Symbol</th><th>Description</th></tr>
<tr><td>1</td><td>SDI</td><td>When IM[3] : Low, Serial in/out signal.
When IM[3] : High, Serial input signal.
The data is applied on the rising edge of the SCL signal.</td></tr>
<tr><td>2</td><td>SDO</td><td>Serial output signal. The data is outputted on the falling edge of the SCL signal.</td></tr>
<tr><td>3
4
5
6</td><td>IM0
IM1
IM2
IM3</td><td>Select the MCU interface mode
<table>
<tr><th rowspan="2">IM3</th><th rowspan="2">IM2</th><th rowspan="2">IM1</th><th rowspan="2">IM0</th><th rowspan="2">MCU-Interface Mode</th><th colspan="2">DB Pin in use</th></tr>
<tr><th>Register/Content</th><th>GRAM</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>80 MCU 8-bit bus interface Ⅰ</td><td>D[7:0]</td><td>D[7:0]</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>80 MCU 16-bit bus interface Ⅰ</td><td>D[7:0]</td><td>D[15:0]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>80 MCU 9-bit bus interface Ⅰ</td><td>D[7:0]</td><td>D[8:0]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>80 MCU 18-bit bus interface Ⅰ</td><td>D[7:0]</td><td>D[17:0]</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>3-wire 9-bit data serial interface Ⅰ</td><td colspan="2">SDA: In/OUT</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>4-wire 8-bit data serial interface Ⅰ</td><td colspan="2">SDA: In/OUT</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>80 MCU 16-bit bus interface Ⅱ</td><td>D[8:1]</td><td>D[17:10], D[8:1]</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>80 MCU 8-bit bus interface Ⅱ</td><td>D[17:10]</td><td>D[17:10]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>80 MCU 18-bit bus interface Ⅱ</td><td>D[8:1]</td><td>D[17:0]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>80 MCU 9-bit bus interface Ⅱ</td><td>D[17:10]</td><td>D[17:9]</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>3-wire 9-bit data serial interface Ⅱ</td><td colspan="2">SDI: In
SDO: Out</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>4-wire 8-bit data serial interface Ⅱ</td><td colspan="2">SDI: In
SDO: Out</td></tr>
</table></td></tr>
<tr><td>7</td><td>RESET</td><td>Reset PIN</td></tr>
<tr><td>8</td><td>VSYNC</td><td>Frame synchronizing signal for RGB interface operation</td></tr>
<tr><td>9</td><td>HSYNC</td><td>Line synchronizing signal for RGB interface operation.</td></tr>
<tr><td>10</td><td>DOTCLK</td><td>Dot clock signal for RGB interface operation.</td></tr>
<tr><td>11</td><td>DE</td><td>Data enable signal for RGB interface operation.</td></tr>
<tr><td>12-29</td><td>DB17-DB0</td><td>18-bit parallel bi-directional data bus for MCU system and RGB interface mode</td></tr>
<tr><td>30</td><td>RDX</td><td>8080-Ⅰ/8080-Ⅱ system (RDX): Serves as a read signal and MCU read data at the rising edge.</td></tr>
<tr><td>31</td><td>WRX</td><td>(WRX) - 8080-Ⅰ/8080-Ⅱ system: Serves as a write signal and writes data at the rising edge.
(D/CX) - 4-line system: Serves as the selector of command or parameter.</td></tr>
<tr><td>32</td><td>DCX</td><td>Display data/command selection pin in parallel interface.
This pin is used to be serial interface clock.
DCX=’1’: display data or parameter. DCX=’0’: command data.
If not used, please fix this pin at VDDI or DGND.</td></tr>
</table>

33	CSX	Chip select input pin (“Low” enable).
34	GND	Power Ground
35	VCI	Power supply
36	IOVCC	Power supply 1.8V-3.3V
37	NC	NC
38	NC	NC
39	LEDK	Backlight LED Cathode
40	LEDA	Backlight LED Anode.

3. Absolute Maximum Ratings

Item	Symbol	MIN	MAX	Unit	Remark
Supply Voltage	V_{DD}	-0.50	+4.6	V	
Supply Voltage(Logic)	V_{DDI}	-0.50	+4.6	V	
Driver Supply Voltage	VGH-VGL	-0.30	+30.0	V	
Operating Temperature	T_{OPR}	-20	70	℃	
Storage Temperature	T_{STG}	-30	80	℃	

4. Electrical Characteristics

4.1 Driving TFT LCD Panel

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Digital Supply Voltage	V_{DD}	2.8	3.0	3.3	V	
TFT Common Electrode	V_{COM}	4.0	4.5	6.4	V	
TFT Gata ON Voltage	V_{GH}	12.2		14.9	V	
TFT Gata ON Voltage	V_{GL}	-12.5		-7.16	V	

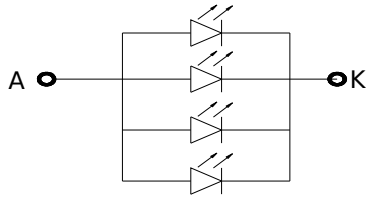
4.2. Driving Backlight

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Forward Current	I_F	-	60	80	mA	Note
Forward Voltage	V_F	2.8	3.1	3.3	V	
Backlight Power consumption	W_{BL}	-	135	-	nW	

Note: 1. The figure below shows the connection of backlight LED.

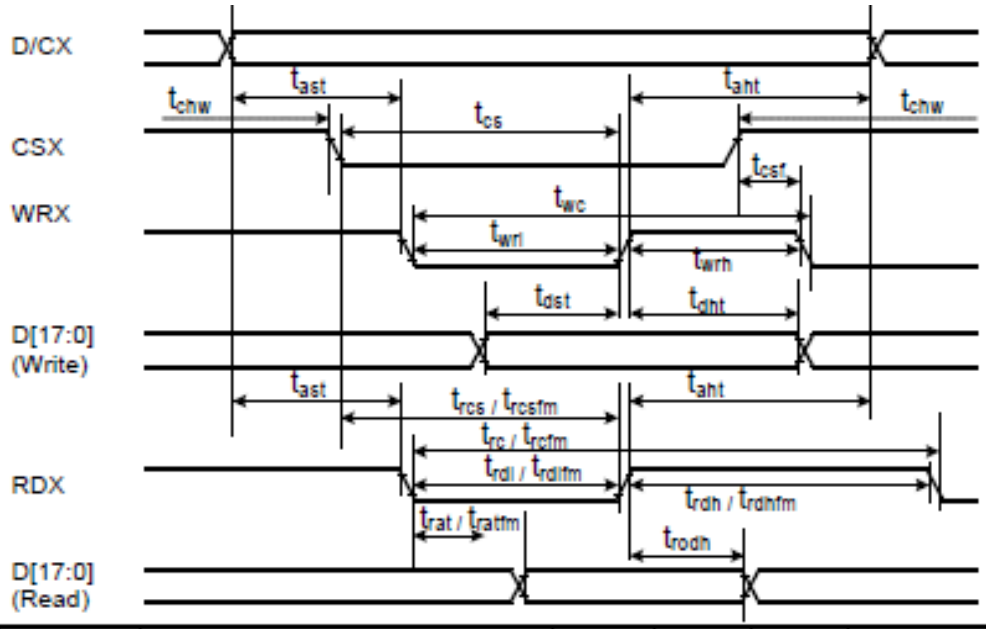
2. One LED: I_F=15mA, V_F=3.1V

3. The lifetime of LED: 50,000 hours



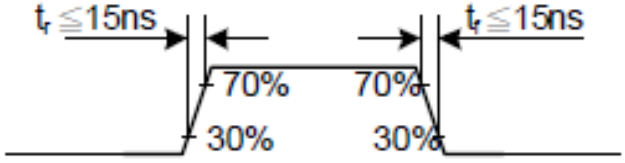
5. Timing Chart

5.1 Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080- Ⅰ system)

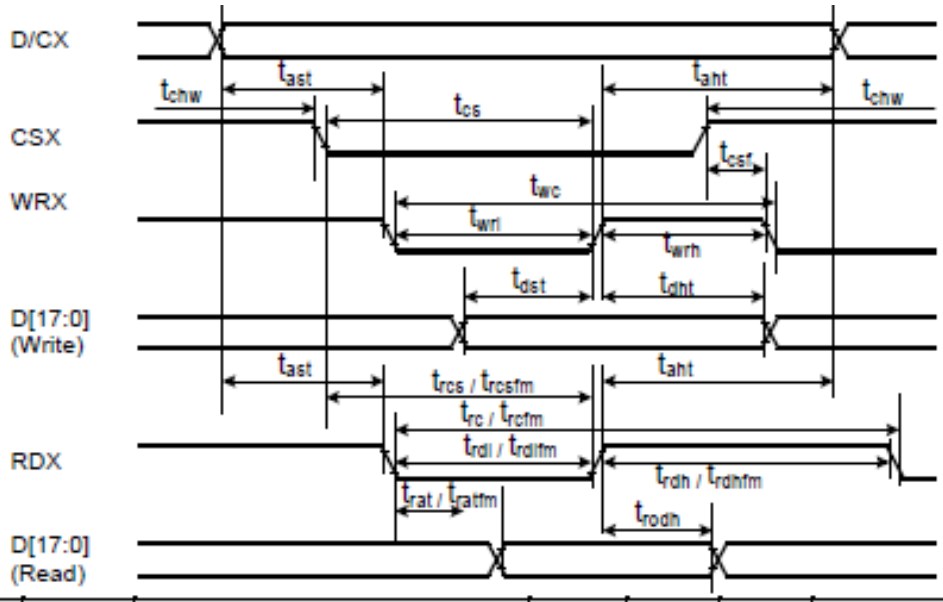


Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time (Write/Read)	0	-	ns	
CSX	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time (Write)	15	-	ns	
	trcs	Chip Select setup time (Read ID)	45	-	ns	
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX (FM)	trcfm	Read Cycle (FM)	450	-	ns	
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
D[17:0], D[15:0], D[8:0], D[7:0]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

Note: Ta = -30 to 70 °C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, VSS=0V

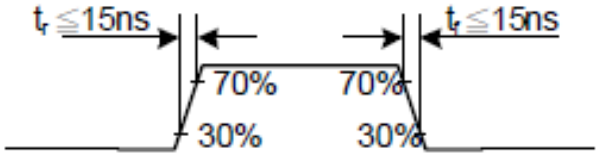


5.2 Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080- Ⅱ system)

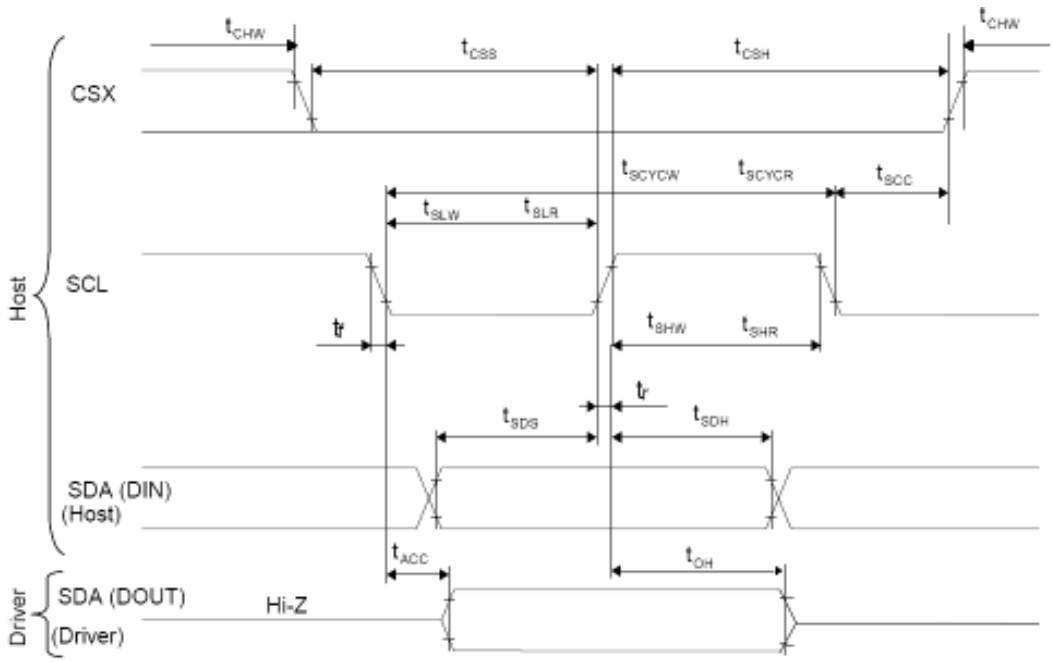


Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time (Write/Read)	0	-	ns	
CSX	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time (Write)	15	-	ns	
	trcs	Chip Select setup time (Read ID)	45	-	ns	
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX (FM)	trcfm	Read Cycle (FM)	450	-	ns	
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
D[17:0], D[17:10]&D[8:1], D[17:10], D[17:9]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

Note: Ta = -30 to 70 °C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, VSS=0V.

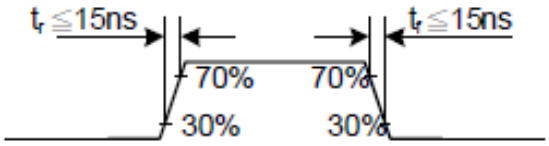


5.3 Display Serial Interface Timing Characteristics (3-line SPI system)

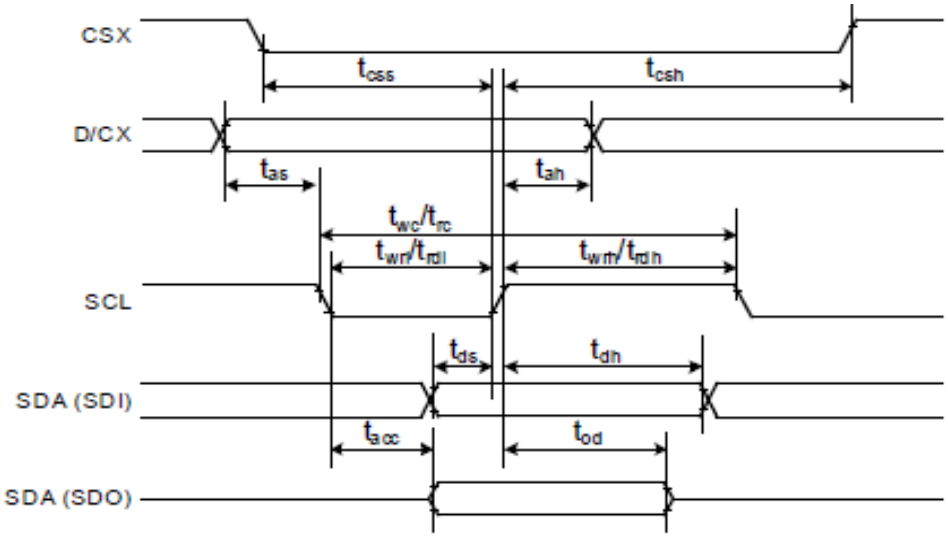


Signal	Symbol	Parameter	min	max	Unit	Description
SCL	tscycw	Serial Clock Cycle (Write)	100	-	ns	
	tshw	SCL "H" Pulse Width (Write)	40	-	ns	
	tslw	SCL "L" Pulse Width (Write)	40	-	ns	
	tscycr	Serial Clock Cycle (Read)	150	-	ns	
	tshr	SCL "H" Pulse Width (Read)	60	-	ns	
	tslr	SCL "L" Pulse Width (Read)	60	-	ns	
SDA / SDI (Input)	tsds	Data setup time (Write)	30	-	ns	
	tsdh	Data hold time (Write)	30	-	ns	
SDA / SDO (Output)	tacc	Access time (Read)	10	-	ns	
	toh	Output disable time (Read)	10	50	ns	
CSX	tscc	SCL-CSX	20	-	ns	
	tchw	CSX "H" Pulse Width	40	-	ns	
	tcss	CSX-SCL Time	60	-	ns	
	tcsh		65	-	ns	

Note: Ta = 25 °C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V

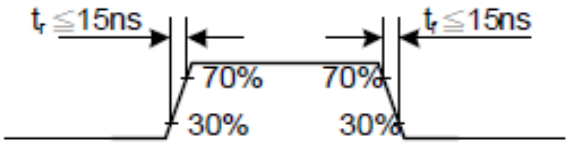


5.4 Display Serial Interface Timing Characteristics (4-line SPI system)

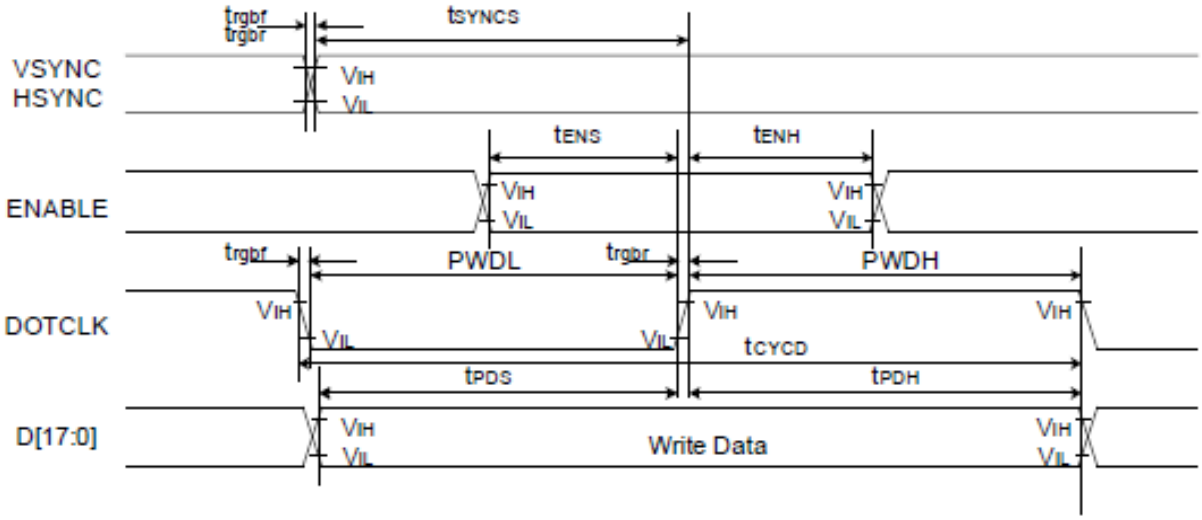


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	40	-	ns	
	tcsh	Chip select hold time (Read)	40	-	ns	
SCL	twc	Serial clock cycle (Write)	100	-	ns	
	twrh	SCL "H" pulse width (Write)	40	-	ns	
	twrl	SCL "L" pulse width (Write)	40	-	ns	
	trc	Serial clock cycle (Read)	150	-	ns	
	trdh	SCL "H" pulse width (Read)	60	-	ns	
	trdl	SCL "L" pulse width (Read)	60	-	ns	
D/CX	tas	D/CX setup time	10	-		
	tah	D/CX hold time (Write / Read)	10	-		
SDA / SDI (Input)	tds	Data setup time (Write)	30	-	ns	
	tdh	Data hold time (Write)	30	-	ns	
SDA / SDO (Output)	taoc	Access time (Read)	10	-	ns	For maximum CL=30pF
	tod	Output disable time (Read)	10	50	ns	For minimum CL=8pF

Note: Ta = 25 °C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V

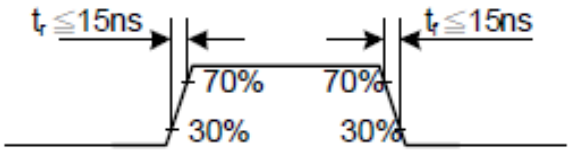


5.5 Parallel 18/16/6-bit RGB Interface Timing Characteristics

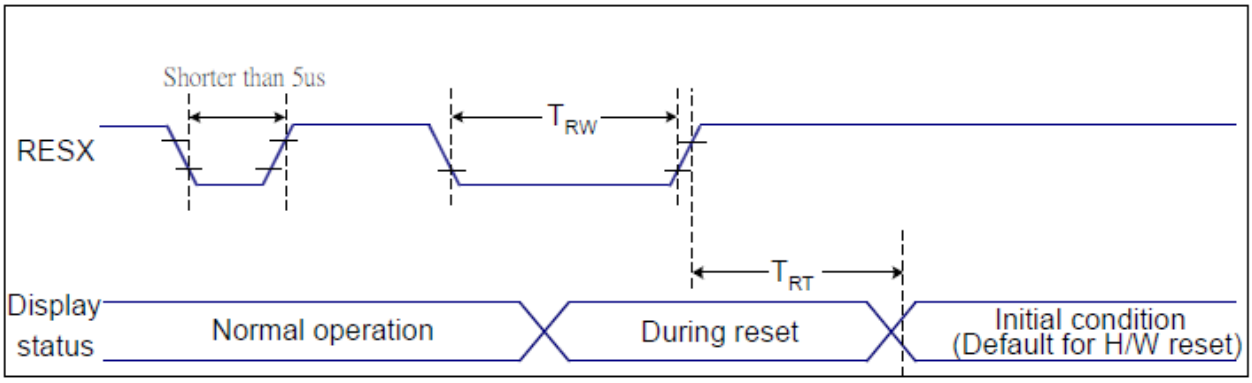


Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	18/16-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t_{ENS}	DE setup time	15	-	ns	
	t_{ENH}	DE hold time	15	-	ns	
D[17:0]	t_{PDS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	15	-	ns	
	PWDL	DOTCLK low-level period	15	-	ns	
	t_{CYCD}	DOTCLK cycle time	100	-	ns	
	t_{rgbr} , t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	6-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t_{ENS}	DE setup time	15	-	ns	
	t_{ENH}	DE hold time	15	-	ns	
D[17:0]	t_{PDS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level pulse period	15	-	ns	
	PWDL	DOTCLK low-level pulse period	15	-	ns	
	t_{CYCD}	DOTCLK cycle time	50	-	ns	
	t_{rgbr} , t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	

Note: Ta = -30 to 70 °C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V



5.6 Reset Timing



Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120 (Note 1, 6, 7)	ms

6. Optical Characteristics

Optical specifications

Items		Symbol	Condition	Specifications			Unit	Remark
				Min.	Typ.	Max.		
Contrast Ratio		CR	θ =0	300	400	-	-	Note
Response Time		T_R	25℃	-	20	30	ms	
		T_F		-	20	30	ms	
Chromaticity	Red	X_R		0.611	0.613	0.615	-	
		Y_R		0.333	0.335	0.337	-	
	Green	X_G		0.305	0.307	0.309	-	
		Y_G		0.558	0.560	0.562	-	
	Blue	X_B		0.133	0.135	0.137	-	
		Y_B		0.158	0.160	0.162	-	
	White	X_W		0.324	0.326	0.328	-	
		Y_W		0.364	0.366	0.368	-	
Viewing angle	Hor.	ϕR(3 o'clock)	Center CR≥10	10	30	-	deg.	
		ϕL(9 o'clock)		10	30	-		
	Ver.	θU(12 o'clock)		10	30	-		
		θD(6 o'clock)		10	15	-		
Uniformity		U		75	80			
NTSC ratio					50		%	
Luminance		Lv		200	250		cd/m^2	

Note 1: Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L63 / L0

L63: Luminance of gray level 63

L0: Luminance of gray level 0

CR = CR (10)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note 5.

Note 2: Definition of Response Time (TR, TF):

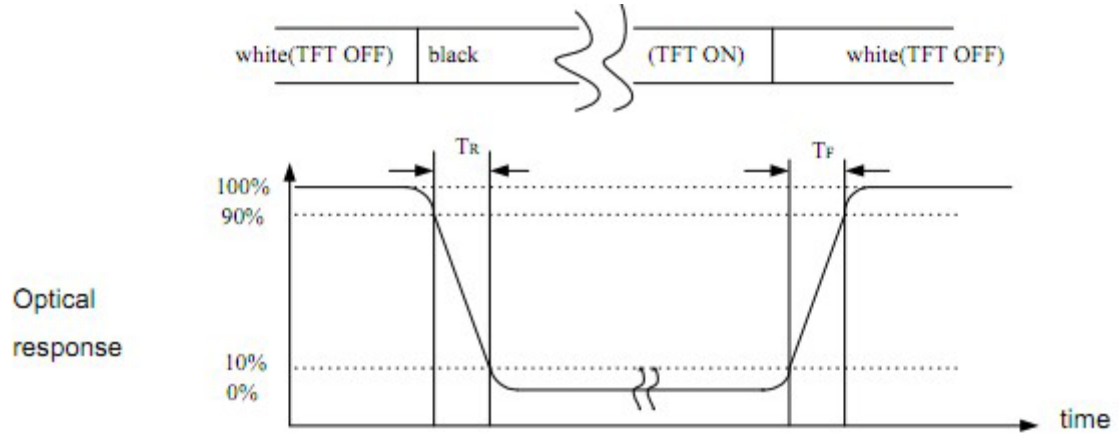


Figure 2

Note 3: Viewing Angle:

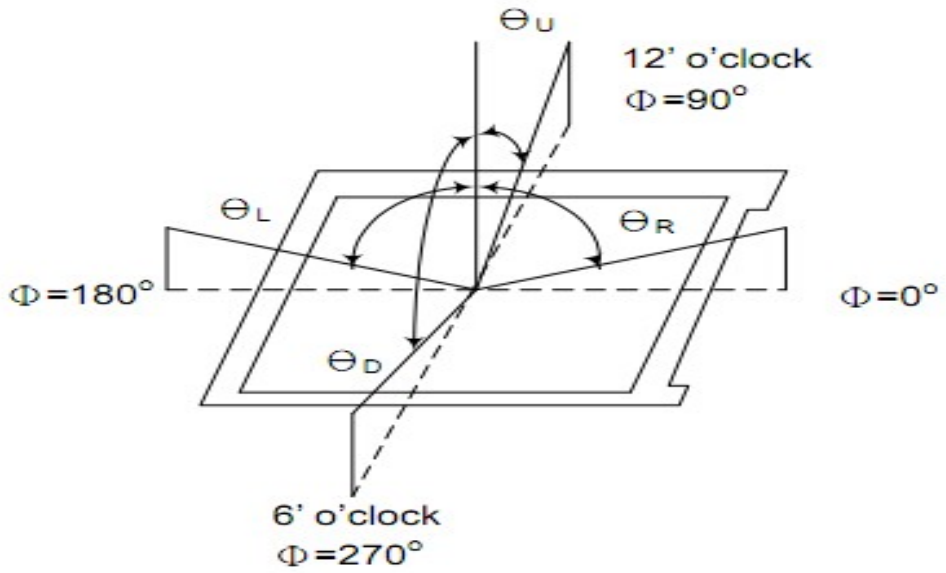


Figure 3

The above "Viewing Angle" is the measuring position with Largest Contrast Ratio; not for good image quality. View Direction for good image quality is 6 O'clock. Module maker can increase the "Viewing Angle" by applying Wide View Film.

Note 4: Measurement Set-Up:

The LCD module should be stabilized at a given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.

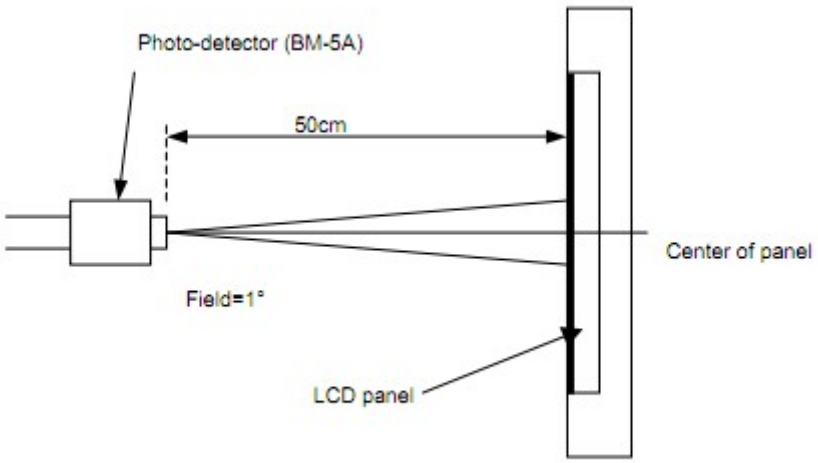


Figure 4

Note 5: Definitions of colder chromaticity (CIE1931)

Color coordinates measured at center point of LCD.

Note 6: Definition of Luminance Uniformity

Active area is divided into 9 measuring areas (Refer Fig.2) Every measuring point is placed at the center of each measuring area.

Luminance Uniformity(U) = Limn/Lmax

L-----Active area length W-----Active area width

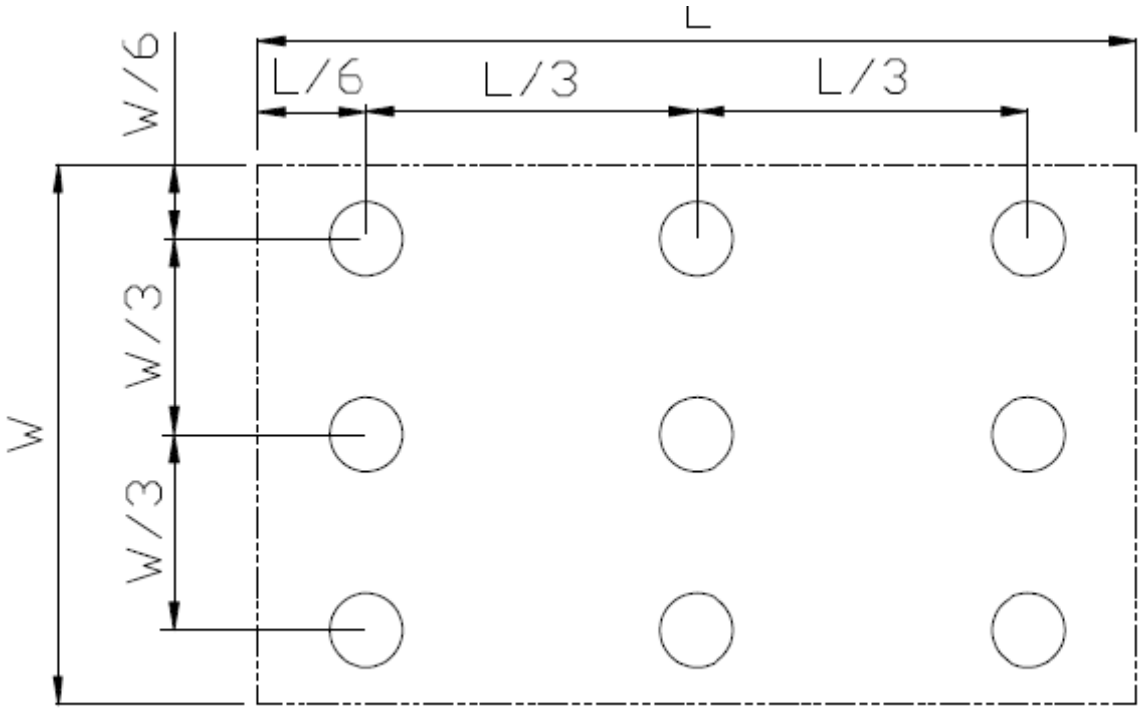


Fig. 2 Definition of uniformity

Lmax: The measured maximum luminance of all measurement position.

Lmin: The measured minimum luminance of all measurement position.

Note 7: Definition of Luminance

Measure the luminance of white state at center point.

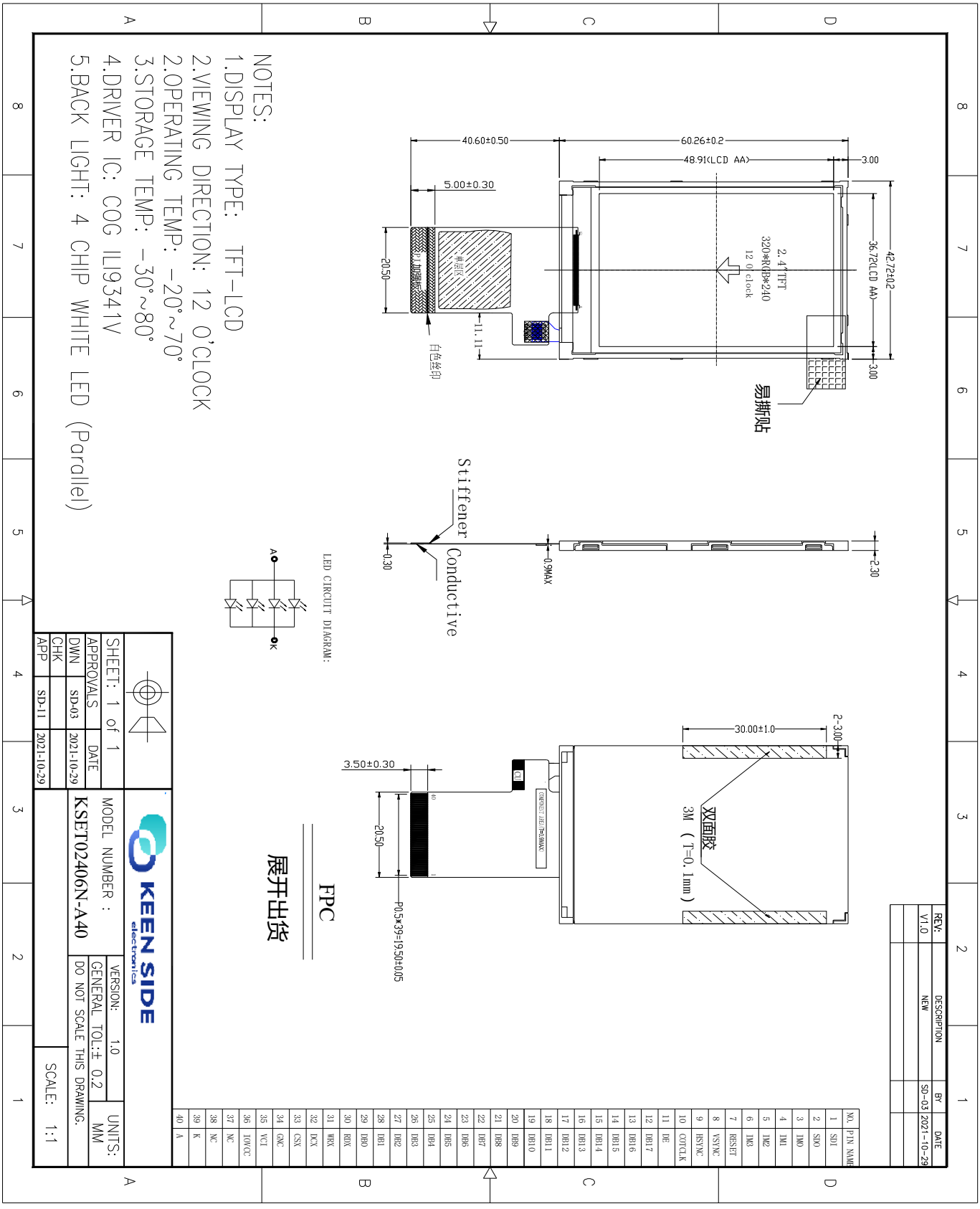
7. Environmental / Reliability Tests

No	Test Item	Condition	Remarks
1	High Temperature Operation	Ts= +70℃, 240hrs	Note 1 IEC60068-2-2, GB2423. 2-89
2	Low Temperature Operation	Ta= -20℃, 240hrs	Note 2 IEC60068-2-1 GB2423.1-89
3	High Temperature Storage	Ta= +80℃, 240hrs	IEC60068-2-2 GB2423. 2-89
4	Low Temperature Storage	Ta= +70℃, 240hrs	IEC60068-2-1 GB/T2423.1-89
5	High Temperature & Humidity Storage	Ta= +60℃, 90% RH max, 160 hours	IEC60068-2-3 GB/T2423.3-2006
6	Thermal Shock (Non-operation)	-30℃ 30 min ~ +80℃ 30 min Change time: 5min, 30 Cycle	Start with cold temperature, end with high temperature IEC60068-2-14, GB2423.22-87
7	Electro Static Discharge (Operation)	C=150pF, R=330 Ω, 5 points/panel Air:±8KV, 5 times; Contact: ±4KV, 5 times; (Environment: 15℃ ~ 35℃, 30% ~ 60%, 86Kpa ~ 106Kpa)	IEC61000-4-2 GB/T17626.2-1998
8	Vibration (Non-operation)	Frequency range: 10~55Hz, Stroke: 1.mm Sweep: 10Hz~55Hz~10Hz 2 hours for each direction of X .Y. Z. (package condition)	IEC60068-2-6 GB/T2423.5-1995
9	Shock (Non-operation)	60G 6ms, ± X, ±Y , ± Z 3 times for each direction	IEC60068-2-27 GB/T2423.5-1995
10	Package Drop Test	Height: 80 cm, 1 corner, 3 edges, 6 surfaces	IEC60068-2-32 GB/T2423.8-1995

Note: 1. T_S is the temperature of panel's surface.

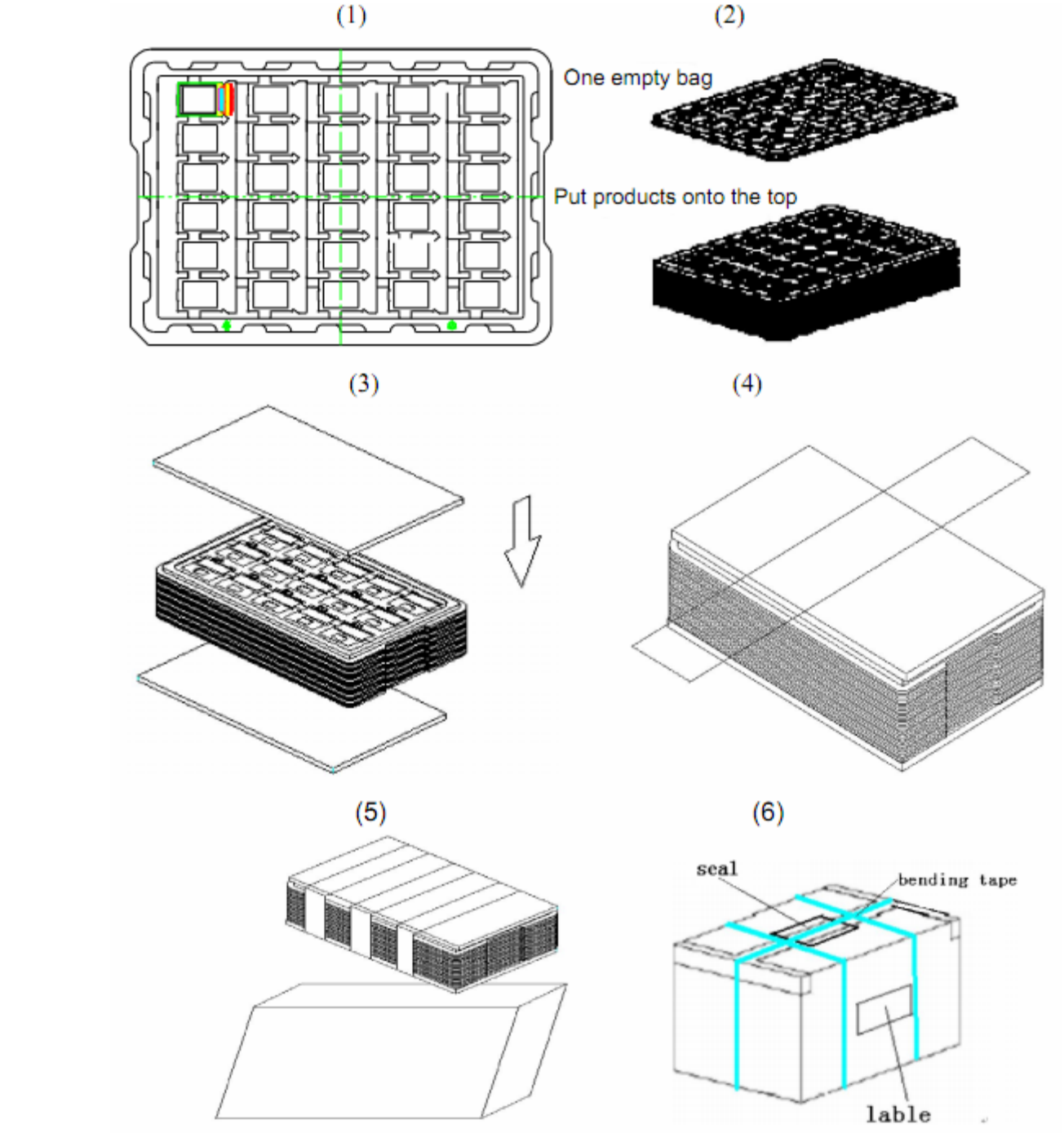
2. Ta is the ambient temperature of sample.

8. Mechanical Drawing



9. Packing

Packing Method



1. Put module into tray cavity:
2. Tray stacking.
3. Put 1 cardboard under the tray stack and 1 cardboard above:
4. Fix the cardboard to the tray stack with adhesive tape:
5. Put the tray stack into carton.
6. Carton sealing with adhesive tape.

10. Precautions for Use of LCD modules

10.1 Handling Precautions

10.1.1. The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

10.1.2. If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

10.1.3. Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

10.1.4. The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

10.1.5. If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

- Isopropyl alcohol
- Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

- Water
- Ketene
- Aromatic solvents

10.1.6. Do not attempt to disassemble the LCD Module.

10.1.7. If the logic circuit power is off, do not apply the input signals.

10.1.8. To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

10.1.8.1. Be sure to ground the body when handling the LCD Modules.

10.1.8.2. Tools required for assembly, such as soldering irons, must be properly ground.

10.1.8.3. To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

10.1.8.4. The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.