SDMX5124

RGB Led Lamp controller

Description

The SDMX5124 is a highly integrated low power single-chip solution for LED light control. It has three PWM channel each of which can provide 4096 colors.

The SDMX5124 use innovation Synchronous DMX512 like protocol SDMX512,which only use one wire when the devices are cascaded (daisy chain configuration),instead SPI BUS use three wire(Data,Clock and LD) and it need not programming ,This character makes the cascade chain more flexible and the chip more easy to use.

The SDMX5124 integrates data sample and align mechanism, phase adapter, shifter, and PWM modules.

Feature

- 1-wire and Clock latched mode.
- CMOS logic, very low power dissipation.
- Few external components
- Integrated phase adapter can make more than 1000 chips in one cascade chain.
- Three LEDs (GREE, RED, BLUE) full color control . And every LED has 16 grade levels. That's let every pixel 4096 colors.
- Output pins with buffer.
- Work voltage.4.5~5.5V
- Low leakage current
- I/O latchup performance: 500 mA
- I/O ESD protection: 2.5 kV HBM
- SOP16 package

Application

Intelligent LED Light controller

Introduction

The SDMX5142 is a highly integrated low power single-chip solution for LED light control. It has Clock latched mode (3 wires) and 1-wire operations mode (only 1 wire). This character makes the cascade chain more flexible and the chip more easy to use. SDMX5142 integrates data sample and align mechanism, phase adapter, shifter, and PWM function modules.

The operation frequency of SDMX5142 can up to 12.288MHZ. And the data transfer rate can be 192Kbit/s.

There are 2 port mode can be configured: clock latched mode and 1-wire mode.
In clock latched mode, 3-wire port valid: data port, synchronous clock port, and system clock port. Serial data is not encoded.
In 1-wire mode, only one port valid: data port. If input mode is 1-wire mode, an external component, Oscillator needed. Serial data is encoded so that the receiver can extract timing information.

Internal frequency relationship:

OSC	MCLK	DLCK	PWM clk
OSC	OSC/32	OSC/64	OSC/32

Example:

OSC	MCLK	DLCK	PWM clk
12.288M	384K	192K	384K
6.144M	192K	96K	192K

Table 1: Frequency relationship

Input and output can be configured to clock latched mode or 1-wire mode independency.
The MODEA configure the input port mode. Please See Table 3.
The MODEB configure the output port mode. Please See Table 4.

Pin description

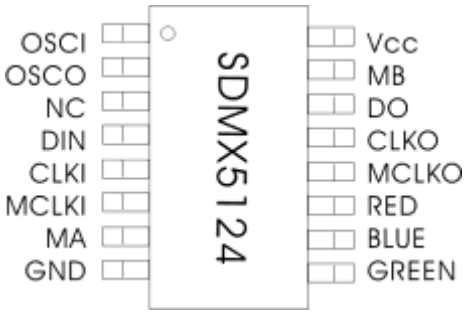


Figure 1 : SDMX5124 Pin Configuration

Pin names	Direction	Description	Comments
DIN	INPUT	Serial data input	
DCLKIN	INPUT	Clock, used to synchronize input serial data	Only used in clock latched mode
MCLKIN	INPUT	System clock source from upper chip	Only used in clock latched mode
DOUT	OUTPUT	Serial data output	Buffered
DCLKOUT	OUTPUT	Clock, used to synchronize output serial data	Buffered
MCLKOUT	OUTPUT	System clock source to lower chip	Buffered
RED	OUTPUT	RED LED PWM control signal	Buffered
GREEN	OUTPUT	GREEN LED PWM control signal	Buffered
BLUE	OUTPUT	BLUE LED PWM control signal	Buffered
MODEA	INPUT	Input data MODE choose	0: 1-wire mode
MODEB	INPUT	Output data MODE choose	1: clock latched mode
OSCIN	INPUT	Oscillator connect pins	
OSCOUT	OUTPUT		

Table 2: Pin description

MODEA	Description	Valid pins
0	Get encoded data from DIN pin	DIN, OSCIN, OSCOUT, RED, GREEN, BLUE
1	Get general binary data from DIN pin	DIN, DCLKIN, MCLKIN, RED, GREEN, BLUE

Table 3: MODEA pin function description

MODEB	Description	Valid pins
0	Send out data after encoded	DOUT
1	Send out data without encoded (General binary code data)	DOUT,DCLKOUT,MCLKOUT

Table 4: MODEB pin function description

Electronic Specification

Recommended Operating Conditions

Symbol	Parameter	Minimum	Maximum	Condition
V_{DD}	Power Supply	4.5v	5.5v	
V_{IL}	Low level input voltage CMOS input CMOS_SCHMITT	 -0.5v -0.5v	 0.2 x VDD 1.25v	Guaranteed input Low Voltage
V_{IH}	High level input voltage CMOS input CMOS_SCHMITT	 0.7 x VDD 2.05v	 VDD + 0.5v VDD + 0.5v	Guaranteed input High Voltage
V_{OL}	Low level output voltage CMOS output		 1.5v	Guaranteed input Low Voltage
V_{OH}	High level output voltage CMOS output	 3.5v		Guaranteed input High Voltage
T_{OP}	Operation Temperature	-20℃	75℃	

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Condition
T_J	Junction Temperature	0℃	125℃	
T_{STG}	Storage Temperature	-65°C	150°C	
$I_{I/O}$	I/O latchup performance	-	500 mA	
V_{ESD}	I/O ESD protection. Electrostatic Discharge Voltage	-	2.5 kV HBM	

Crystal Oscillator for SDMX5124

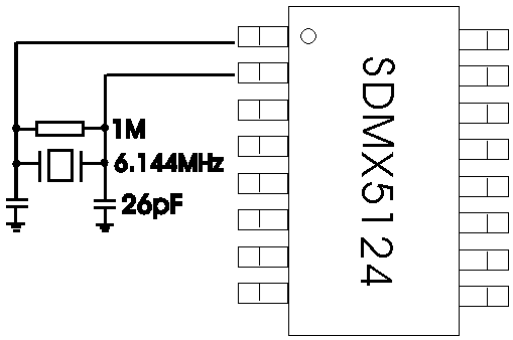
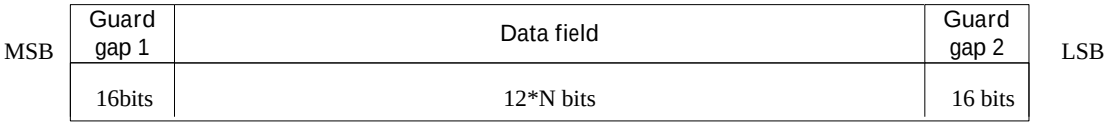


Figure 2: Oscillator configuration

Function description

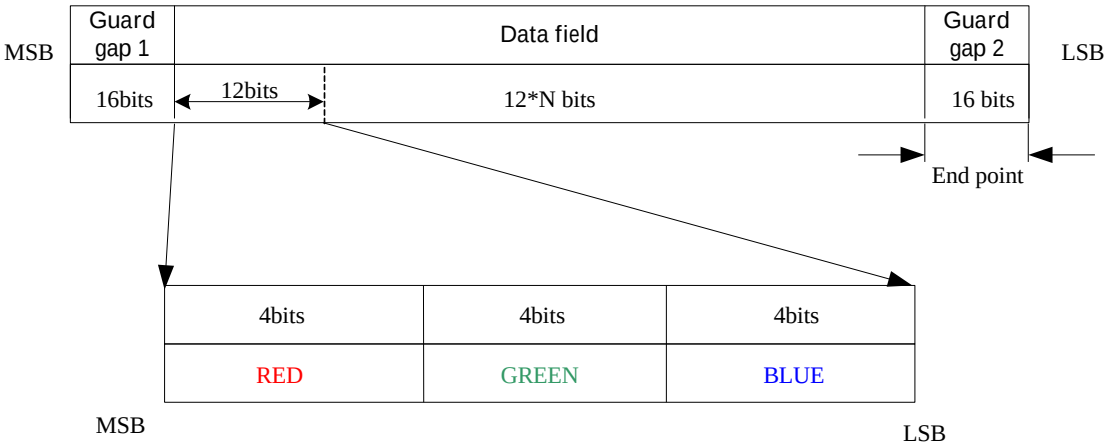
1. Data frame structure

Frame structure:



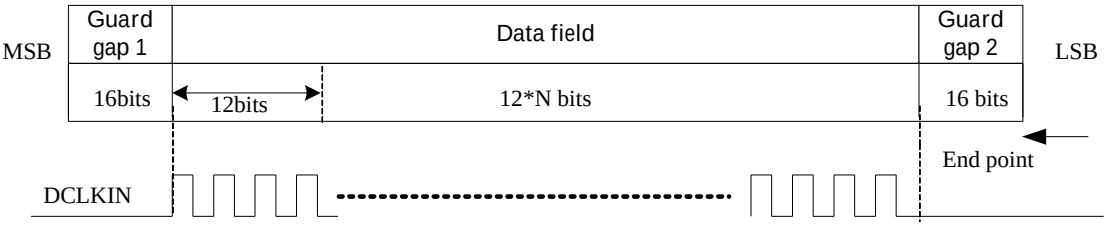
*Note: N is number of pixel

If OSC=12.288MHZ or MCLK=384KHZ, one SDMX5124 cascade chain can control (192000-16-16)/12= 15997 pixels according to the frame structure in one second. Or drive 512 pixels 192000/（16*2+12*512）=30 times/s.



*Note: N is number of pixel

In 1-wire mode, DCLKIN will keep unchanged tile data field.



*Note: N is number of pixel

Input signals relationship: Clock latched mode

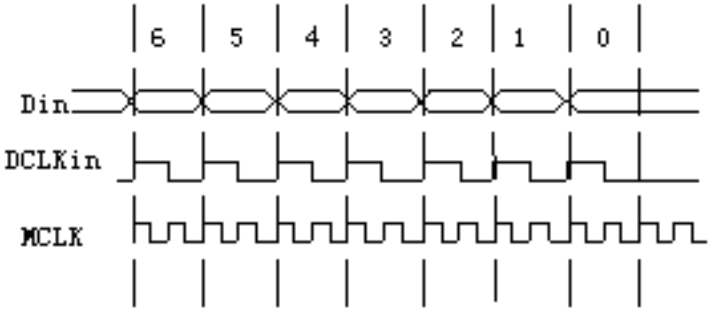
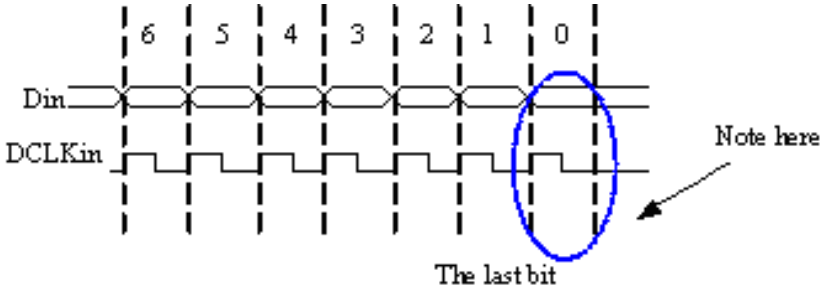


Figure 3: Timing of Clock latched mode signals

*Note:
When receiving port in Clock latched mode, the DCLKin cycle of last bit should be completed, 50% high and 50% low.



The timing relationship sees below:

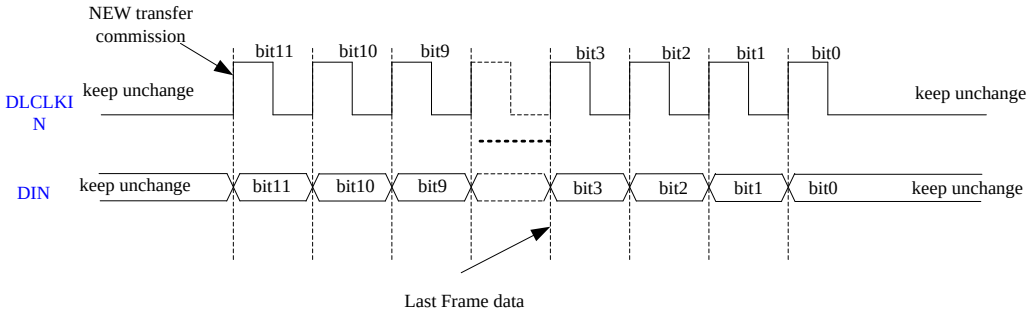


Figure 4: General serial data timing relationship

Input signals timing relationship: 1-wire mode

For only 1 wire communication, no special note in this mode.

There are there 4-bit registers control the LED flash duty cycle. The relationship between LED light and LED control register value see below:

LED value 4 bits	Description		
	Number of '1'	Number of '0'	Duty cycle
0	0	16	0
1	1	15	1/15
2	2	14	2/14
3	3	13	3/13
4	4	12	4/12

5	5	11	5/11
6	6	10	6/10
7	7	9	7/9
8	8	8	8/8
9	9	7	9/7
10	10	6	10/6
11	11	5	11/5
12	12	4	12/4
13	13	3	13/3
14	14	2	14/2
15	16	0	1

The PWM period of LED is 26.05us (OSC=12.288MHZ or MCLKIN=384KHZ) or 52.08us (OSC=6.144MHZ or MCLKIN=192KHZ)。

Cascade chain

The SDMX5124 can build the cascade chain flexible. Every SDMX5124 has 2 choose: Clock latched mode or 1-wire port mode. And the input and output can choose the data mode independently.

The data port mode is configured by the MODEA and MODEB pins.

If configure the DMX5124 input port to 1-wire mode, it need an OSC to support the system source clock.

Cascade chain description:

Clock latched mode connection (general binary data format):

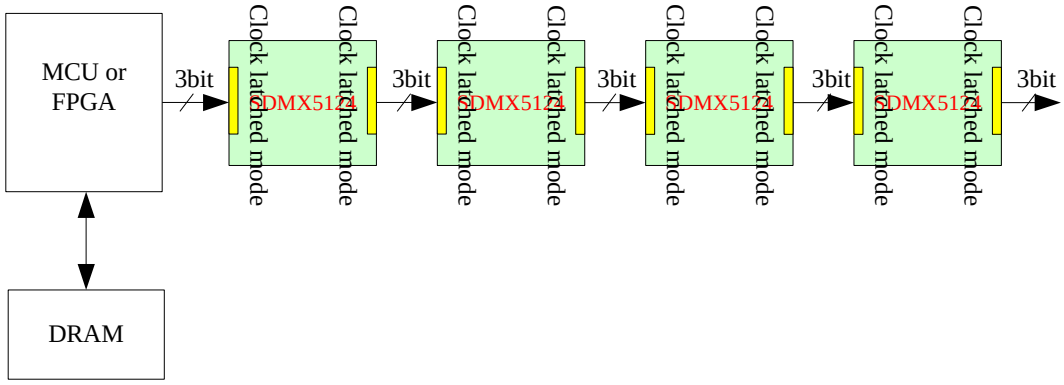


Figure 5: Clock latched mode chain

1-wire mode (Encoded serial data port)

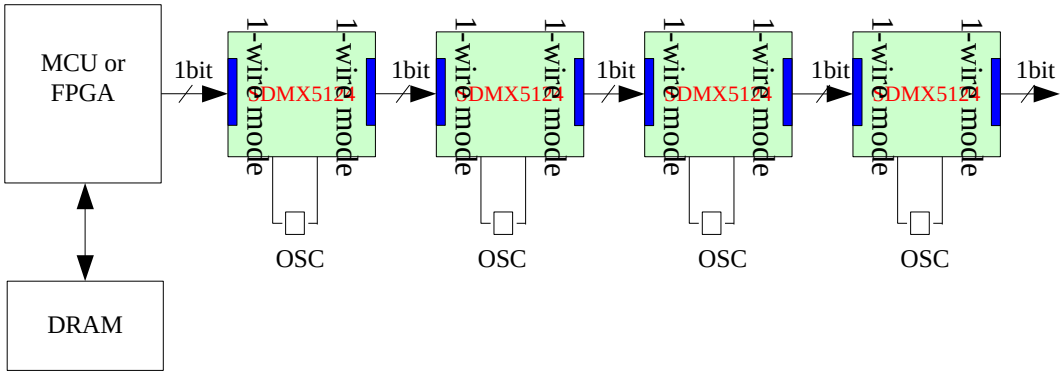


Figure 6: 1-wire mode chain

Mixed with 1-wire mode and Clock latched mode as your wish.

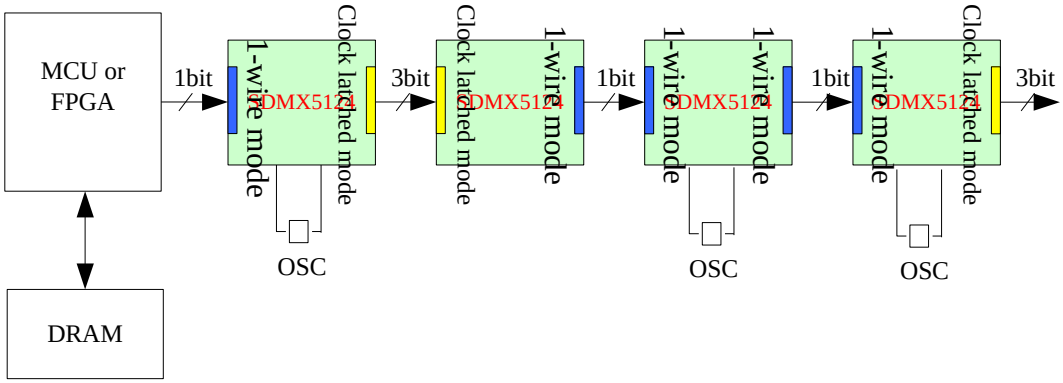


Figure 7: Mix mode chain

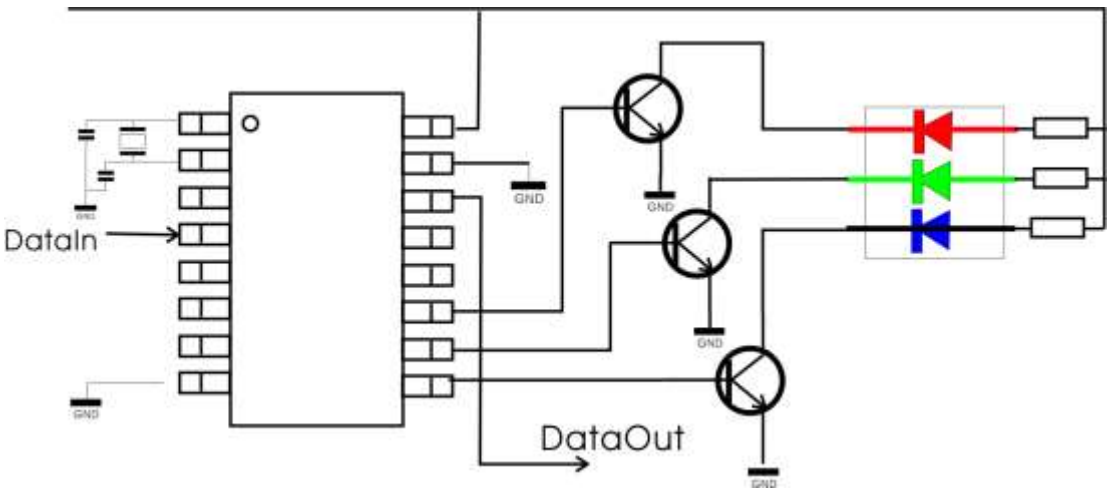
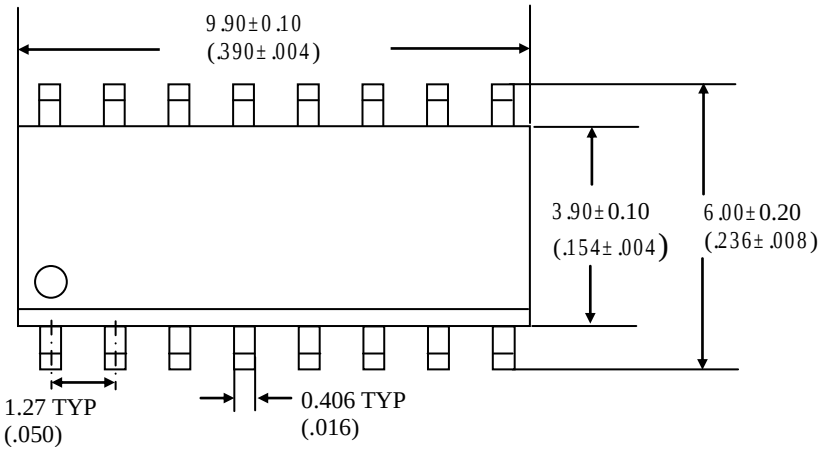
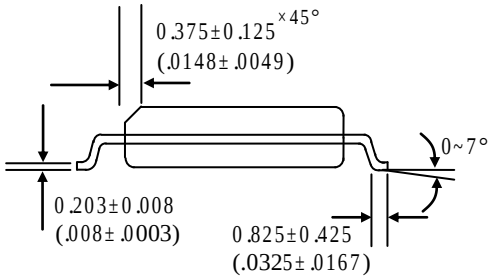


Figure 8: Typical Application

Package Information

Figure 9: SOP16 package





Lead Pitch	1.27mm(50mil)
Trim Flange	0~0.1mm(0~3.9mil)
Unit	mm(inches)
Pad Size	90mil x 110mil
	90mil x 130mil
	95mil x 180mil