bq20z655-R1 SBS 1.1-Compliant Gas Gauge and Protection Enabled With Impedance Track™

1 Features

- Next Generation Patented Impedance Track™ Technology Accurately Measures Available Charge in Li-Ion and Li-Polymer Batteries
  - Better Than 1% Error Over the Lifetime of the Battery
- Supports Smart Battery Specification SBS V1.1
- Flexible Configuration for 2-Series to 4-Series Li-Ion and Li-Polymer Cells
- Powerful 8-Bit RISC CPU with Ultralow Power Modes
- Full Array of Programmable Protection Features
  - Voltage, Current, and Temperature
- Satisfies JEITA Guidelines
- Added Flexibility to Handle More Complex Charging Profiles
- Lifetime Data Logging
- Drives 3, 4, or 5 Segment Liquid Crystal Display and LED for Battery-Pack Conditions
- Supports SHA-1 Authentication
- Complete Battery Protection and Gas Gauge Solution in One Package

2 Applications

- Medical and Test Equipment
- Portable Instrumentation and Industrial Equipment
- Rechargeable Battery Packs

3 Description

The bq20z655-R1 SBS-compliant gas gauge and protection IC, incorporating patented Impedance Track™ technology, is a single IC solution designed for battery-pack or in-system installation. The bq20z655-R1 measures and maintains an accurate record of available charge in Li-ion or Li-polymer batteries using its integrated high-performance analog peripherals. The bq20z655-R1 monitors capacity change, battery impedance, open-circuit voltage, and other critical parameters of the battery pack which reports the information to the system host controller over a serial-communication bus. Together with the integrated analog front-end (AFE) short circuit and overload protection, the bq20z655-R1 maximizes functionality and safety while minimizing external component count, cost, and size in smart battery circuits.

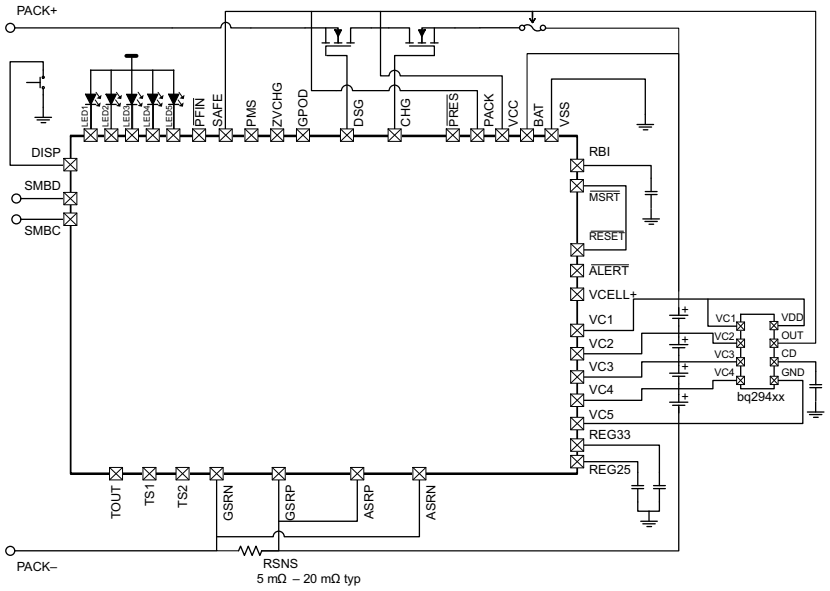
The implemented Impedance Track™ gas gauging technology continuously analyzes the battery impedance, resulting in superior gas-gauging accuracy. This enables remaining capacity to be calculated with discharge rate, temperature, and cell aging all accounted for during each stage of every cycle with high accuracy.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
bq20z655-R1	DBT (44)	4.40 mm × 11.29 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

System Partitioning Diagram



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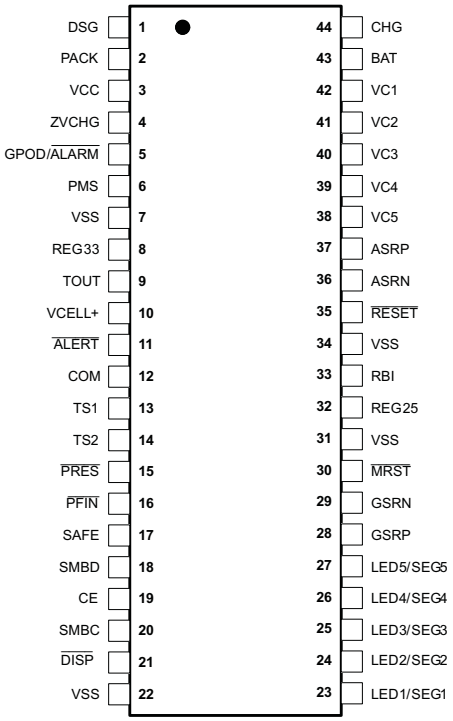
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (August 2011) to Revision A	Page
• *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Deleted "Charge Enable (CE) Affects the Normal Operation on the Charge FET when the Battery Is in Charge/Relax Mode" from *Features*	1

5 Pin Configuration and Functions

DBT Package
44-Pin TSSOP
Top View



Pin Functions

PIN		I/O(1)	DESCRIPTION
NO.	NAME		
1	DSG	O	High side N-chan discharge FET gate drive
2	PACK	IA, P	Battery pack input voltage sense input. It also serves as device wakeup when device is in shutdown mode.
3	VCC	P	Positive device supply input. Connect to the center connection of the CHG FET and DSG FET to ensure device supply either from battery stack or battery pack input
4	ZVCHG	O	P-chan pre-charge FET gate drive
5	GPOD	OD	High voltage general purpose open drain output. Can be configured to be used in pre-charge condition
6	PMS	I	Pre-charge mode setting input. Connect to PACK to enable 0-V precharge using charge FET connected at CHG pin. Connect to VSS to disable 0-V precharge using charge FET connected at CHG pin.
7	VSS	P	Negative supply voltage input. Connect all VSS pins together for operation of device
8	REG33	P	3.3-V regulator output. Connect at least a 2.2-μF capacitor to REG33 and VSS
9	TOUT	P	Thermistor bias supply output
10	VCELL+	—	Internal cell voltage multiplexer and amplifier output. Connect a 0.1-μF capacitor to VCELL+ and VSS
11	$\overline{\text{ALERT}}$	OD	Alert output. In case of short circuit condition, overload condition and watchdog time out this pin will be triggered.
12	COM/TP	—	Output / open drain: LCD common connection
13	TS1	IA	1st Thermistor voltage input connection to monitor temperature
14	TS2	IA	2nd Thermistor voltage input connection to monitor temperature

(1) I = Input, IA = Analog input, I/O = Input/output, I/OD = Input/Open-drain output, O = Output, OA = Analog output, P = Power

Pin Functions (continued)

PIN		I/O(1)	DESCRIPTION
NO.	NAME		
15	$\overline{\text{PRES}}$	I	Active low input to sense system insertion. Typically requires additional ESD protection.
16	$\overline{\text{PFIN}}$	I	Active low input to detect secondary protector status, and to allow the bq20z655-R1 to report the status of the 2nd level protection input.
17	SAFE	OD	Active high output to enforce additional level of safety protection; for example, fuse blow.
18	SMBD	I/OD	SMBus data open-drain bidirectional pin used to transfer address and data to and from the bq20z655-R1
19	CE	—	A logical high on this pin only affects the normal operation on the charge FET when the battery is in charge/relax mode. For a logic low, the normal bq20z655-R1 firmware controls the charge FET.
20	SMBC	I/OD	SMBus clock open-drain bidirectional pin used to clock the data transfer to and from the bq20z655-R1
21	$\overline{\text{DISP}}$	I	Input: In LED mode, this is the display enable input.
22	VSS	P	Negative supply voltage input. Connect all VSS pins together for operation of device
23	LED1/SEG1	I	Output / open drain: LED 1 current sink. LCD segment 1
24	LED2/SEG2	I	Output / open drain: LED 2 current sink. LCD segment 2
25	LED3/SEG3	I	Output / open drain: LED 3 current sink. LCD segment 3
26	LED4/SEG4	I	Output / open drain: LED 4 current sink. LCD segment 4
27	LED5/SEG5	I	Output / open drain: LED 5 current sink. LCD segment 5
28	GSRP	IA	Coulomb counter differential input. Connect to one side of the sense resistor
29	GSRN	IA	Coulomb counter differential input. Connect to one side of the sense resistor
30	$\overline{\text{MRST}}$	I	Master reset input that forces the device into reset when held low. Must be held high for normal operation. Connect to $\overline{\text{RESET}}$ for correct operation of device
31	VSS	P	Negative supply voltage input. Connect all VSS pins together for operation of device
32	REG25	P	2.5-V regulator output. Connect at least a 1-mF capacitor to REG25 and VSS
33	RBI	P	RAM / Register backup input. Connect a capacitor to this pin and VSS to protect loss of RAM/Register data in case of short circuit condition.
34	VSS	P	Negative supply voltage input. Connect all VSS pins together for operation of device
35	$\overline{\text{RESET}}$	O	Reset output. Connect to $\overline{\text{MSRT}}$.
36	ASRN	IA	Short circuit and overload detection differential input. Connect to sense resistor
37	ASRP	IA	Short circuit and overload detection differential input. Connect to sense resistor
38	VC5	IA, P	Cell voltage sense input and cell balancing input for the negative voltage of the bottom cell in cell stack.
39	VC4	IA, P	Cell voltage sense input and cell balancing input for the positive voltage of the bottom cell and the negative voltage of the second lowest cell in cell stack.
40	VC3	IA, P	Cell voltage sense input and cell balancing input for the positive voltage of the second lowest cell in cell stack and the negative voltage of the second highest cell in 4 cell applications.
41	VC2	IA, P	Cell voltage sense input and cell balancing input for the positive voltage of the second highest cell and the negative voltage of the highest cell in 4 cell applications. Connect to VC3 in 2 cell stack applications.
42	VC1	IA, P	Cell voltage sense input and cell balancing input for the positive voltage of the highest cell in cell stack in 4 cell applications. Connect to VC2 in 2- or 3-stack applications.
43	BAT	I, P	Battery stack voltage sense input.
44	CHG	O	High side N-channel charge FET gate drive

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{SS}	Supply voltage	BAT, VCC	–0.3	34	V
		PACK, PMS	–0.3	34	
		VC(n)–VC(n+1); n = 1, 2, 3, 4	–0.3	8.5	
		VC1, VC2, VC3, VC4	–0.3	34	
		VC5	–0.3	1	
V_{IN}	Input voltage	$\overline{PFIN}$, SMBD, SMBC. LED1, LED2, LED3, LED4, LED5, $\overline{DISP}$	–0.3	6	V
		TS1, TS2, SAFE, VCELL+, $\overline{PRES}$, $\overline{ALERT}$	–0.3	$V_{(REG25)}$ + 0.3	
		$\overline{MRST}$, GSRN, GSRP, RBI	–0.3	$V_{(REG25)}$ + 0.3	
		ASRN, ASRP	–1	1	
V_{OUT}	Output voltage	DSG, CHG, GPOD	–0.3	34	V
		ZVCHG	–0.3	$V_{(BAT)}$	
		TOUT, $\overline{ALERT}$, REG33	–0.3	6	
		$\overline{RESET}$	–0.3	7	
		REG25	–0.3	2.75	
I_{SS}	Maximum combined sink current for input pins	$\overline{PRES}$, $\overline{PFIN}$, SMBD, SMBC, LED1, LED2, LED3, LED4, LED5		50	mA
T_A	Operating free-air temperature		–40	85	°C
T_F	Functional temperature		–40	100	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{SS}	Supply voltage	VCC, BAT	4.5		25	V
$V_{(STARTUP)}$	Minimum start-up voltage	VCC, BAT, PACK	5.5			V
V_{IN}	Input voltage	VC(n)-VC(n+1); n = 1,2,3,4	0		5	V
		VC1, VC2, VC3, VC4	0		V_{SS}	V
		VC5	0		0.5	V
		ASRN, ASRP	–0.5		0.5	V
		PACK, PMS	0		25	V
$V_{(GPOD)}$	Output voltage	GPOD	0		25	V
$I_{(GPOD)}$	Drain current(1)	GPOD			1	mA
$C_{(REG25)}$	2.5-V LDO capacitor	REG25	1			µF
$C_{(REG33)}$	3.3-V LDO capacitor	REG33	2.2			µF
$C_{(VCELL+)}$	Cell voltage output capacitor	VCELL+	0.1			µF
$R_{(PACK)}$	PACK input block resistor(2)	PACK	1			kΩ

(1) Use an external resistor to limit the current to GPOD to 1 mA in high voltage application.
(2) Use an external resistor to limit the inrush current PACK pin required.

6.4 Thermal Information

THERMAL METRIC[1]		bq20z655-R1 DBT (TSSOP) 44 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	60.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	15.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	30.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	27.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Over operating free-air temperature range, T_A = –40°C to 85°C, $V_{(REG25)}$ = 2.41 V to 2.59 V, $V_{(BAT)}$ = 14 V, $C_{(REG25)}$ = 1 µF, $C_{(REG33)}$ = 2.2 µF; typical values at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
$I_{(NORMAL)}$	Firmware running			550		µA
$I_{(SLEEP)}$	Sleep mode	CHG FET on; DSG FET on		124		µA
		CHG FET off; DSG FET on		90		µA
		CHG FET off; DSG FET off		52		µA
$I_{(SHUTDOWN)}$	Shutdown mode			0.1	1	µA
SHUTDOWN WAKE; T_A = 25°C (unless otherwise noted)						
$I_{(PACK)}$	Shutdown exit at $V_{STARTUP}$ threshold				1	µA
SRx WAKE FROM SLEEP; T_A = 25°C (unless otherwise noted)						
$V_{(WAKE)}$	Positive or negative wake threshold with 1-mV, 2.25-mV, 4.5-mV and 9-mV programmable options		1.25		10	mV
$V_{(WAKE\_ACR)}$	Accuracy of $V_{(WAKE)}$	$V_{(WAKE)}$ = 1 mV; $I_{(WAKE)}$= 0, RSNS1 = 0, RSNS0 = 1;	–0.7		0.7	mV
		$V_{(WAKE)}$ = 2.25 mV; $I_{(WAKE)}$) = 1, RSNS1 = 0, RSNS0 = 1; $I_{(WAKE)}$ = 0, RSNS1 = 1, RSNS0 = 0;	–0.8		0.8	
		$V_{(WAKE)}$ = 4.5 mV; $I_{(WAKE)}$ = 1, RSNS1 = 1, RSNS0 = 1; $I_{(WAKE)}$ = 0, RSNS1 = 1, RSNS0 = 0;	–1		1	
		$V_{(WAKE)}$ = 9 mV; $I_{(WAKE)}$ = 1, RSNS1 = 1, RSNS0 = 1;	–1.4		1.4	
$V_{(WAKE\_TCO)}$	Temperature drift of $V_{(WAKE)}$ accuracy			0.5		%/°C
$t_{(WAKE)}$	Time from application of current and wake of bq20z655-R1			1	10	ms
WATCHDOG TIMER						
t_{WDTINT}	Watchdog start-up detect time		250	500	1000	ms
t_{WDWT}	Watchdog detect time		50	100	150	µs
2.5V LDO; $I_{(REG33OUT)}$ = 0 mA; T_A = 25°C (unless otherwise noted)						
$V_{(REG25)}$	Regulator output voltage	4.5 < VCC or BAT < 25 V; $I_{(REG25OUT)}$) ≤ 16 mA; T_A = –40°C to 100°C	2.41	2.5	2.59	V
$\Delta V_{(REG25TEMP)}$	Regulator output change with temperature	$I_{(REG25OUT)}$ = 2 mA; T_A = –40°C to 100°C		±0.2%		
$\Delta V_{(REG25LINE)}$	Line regulation	5.4 < VCC or BAT < 25 V; $I_{(REG25OUT)}$ = 2 mA		3	10	mV
$\Delta V_{(REG25LOAD)}$	Load regulation	0.2 mA ≤ $I_{(REG25OUT)}$ ≤ 2 mA		7	25	mV
		0.2 mA ≤ $I_{(REG25OUT)}$ ≤ 16 mA		25	50	
$I_{(REG25MAX)}$	Current limit	drawing current until REG25 = 2 V to 0 V	5	40	75	mA
3.3V LDO; $I_{(REG25OUT)}$ = 0 mA; T_A = 25°C (unless otherwise noted)						

Electrical Characteristics (continued)

Over operating free-air temperature range, T_A = –40°C to 85°C, $V_{(REG25)}$ = 2.41 V to 2.59 V, $V_{(BAT)}$ = 14 V, $C_{(REG25)}$ = 1 µF, $C_{(REG33)}$ = 2.2 µF; typical values at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(REG33)}$	Regulator output voltage	4.5 < VCC or BAT < 25 V; $I_{(REG33OUT)}$ ≤ 25 mA; T_A = –40°C to 100°C	3	3.3	3.6	V
$\Delta V_{(REG33TEMP)}$	Regulator output change with temperature	$I_{(REG33OUT)}$ = 2 mA; T_A = –40°C to 100°C		±0.2%		
$\Delta V_{(REG33LINE)}$	Line regulation	5.4 < VCC or BAT < 25 V; $I_{(REG33OUT)}$ = 2 mA		3	10	mV
$\Delta V_{(REG33LOAD)}$	Load regulation	0.2 mA ≤ $I_{(REG33OUT)}$ ≤ 2 mA		7	17	mV
		0.2 mA ≤ $I_{(REG33OUT)}$ ≤ 25 mA		40	100	
$I_{(REG33MAX)}$	Current limit	drawing current until REG33 = 3 V	25	100	145	mA
		short REG33 to VSS, REG33 = 0 V	12		65	
THERMISTOR DRIVE						
$V_{(TOUT)}$	Output voltage	$I_{(TOUT)}$ = 0 mA; T_A = 25°C		$V_{(REG25)}$		V
$R_{DS(on)}$	TOUT pass element resistance	$I_{(TOUT)}$ = 1 mA; $R_{DS(on)}$ = ($V_{(REG25)}$ - $V_{(TOUT)}$)/ 1 mA; T_A = –40°C to 100°C		50	100	Ω
LED OUTPUTS						
V_{OL}	Output low voltage	LED1, LED2, LED3, LED4, LED5			0.4	V
VCELL+ HIGH VOLTAGE TRANSLATION						
$V_{(VCELL+OUT)}$	Translation output	VC(n) - VC(n+1) = 0 V; T_A = –40°C to 100°C	0.95	0.975	1	V
		VC(n) - VC(n+1) = 4.5 V; T_A = –40°C to 100°C	0.275	0.3	0.375	
$V_{(VCELL+REF)}$		Internal AFE reference voltage ; T_A = –40°C to 100°C	0.965	0.975	0.985	
$V_{(VCELL+PACK)}$		Voltage at PACK pin; T_A = –40°C to 100°C	0.98 × $V_{(PACK)}$/18	$V_{(PACK)}$/18	1.02 × $V_{(PACK)}$/18	
$V_{(VCELL+BAT)}$		Voltage at BAT pin; T_A = –40°C to 100°C	0.98 × $V_{(BAT)}$/18	$V_{(BAT)}$/18	1.02 × $V_{(BAT)}$/18	
CMMR	Common mode rejection ratio	VCELL+	40			dB
K	Cell scale factor	K= {VCELL+ output (VC5=0 V; VC4=4.5 V) - VCELL+ output (VC5=0 V; VC4=0 V)}/4.5	0.147	0.15	0.153	
		K= {VCELL+ output (VC2=13.5 V; VC1=18 V) - VCELL+ output (VC5=13.5 V; VC1=13.5 V)}/4.5	0.147	0.15	0.153	
$I_{(VCELL+OUT)}$	Drive Current to VCELL+ capacitor	VC(n) - VC(n+1) = 0 V; VCELL+ = 0 V; T_A = –40°C to 100°C	12	18		µA
$V_{(VCELL+O)}$	CELL offset error	CELL output (VC2 = VC1 = 18 V) - CELL output (VC2 = VC1 = 0 V)	–18	–1	18	mV
I_{VCnL}	VC(n) pin leakage current	VC1, VC2, VC3, VC4, VC5 = 3 V	–1	0.01	1	µA
CELL BALANCING						
R_{BAL}	internal cell balancing FET resistance	$R_{DS(on)}$ for internal FET switch at V_{DS} = 2 V; T_A = 25°C	200	400	600	Ω
HARDWARE SHORT CIRCUIT AND OVERLOAD PROTECTION; T_A = 25°C (unless otherwise noted)						
$V_{(OL)}$	OL detection threshold voltage accuracy	V_{OL} = 25 mV (minimum)	15	25	35	mV
		V_{OL} = 100 mV; RSNS = 0, 1	90	100	110	
		V_{OL} = 205 mV (maximum)	185	205	225	
$V_{(SCC)}$	SCC detection threshold voltage accuracy	$V_{(SCC)}$ = 50 mV (minimum)	30	50	70	mV
		$V_{(SCC)}$ = 200 mV; RSNS = 0, 1	180	200	220	
		$V_{(SCC)}$ = 475 mV (maximum)	428	475	523	
$V_{(SCD)}$	SCD detection threshold voltage accuracy	$V_{(SCD)}$ = –50 mV (minimum)	–30	–50	–70	mV
		$V_{(SCD)}$ = –200 mV; RSNS = 0, 1	–180	–200	–220	
		$V_{(SCD)}$ = –475 mV (maximum)	–428	–475	–523	
t_{da}	Delay time accuracy			±15.25		µs
t_{pd}	Protection circuit propagation delay			50		µs
FET DRIVE CIRCUIT; T_A = 25°C (unless otherwise noted)						

Electrical Characteristics (continued)

Over operating free-air temperature range, T_A = –40°C to 85°C, $V_{(REG25)}$ = 2.41 V to 2.59 V, $V_{(BAT)}$ = 14 V, $C_{(REG25)}$ = 1 µF, $C_{(REG33)}$ = 2.2 µF; typical values at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(DSGON)}$	DSG pin output on voltage	$V_{(DSGON)} = V_{(DSG)} - V_{(PACK)}$; $V_{(GS)}$ connected to 10 MΩ; DSG and CHG on; T_A = –40°C to 100°C		8	12	16	V
$V_{(CHGON)}$	CHG pin output on voltage	$V_{(CHGON)} = V_{(CHG)} - V_{(BAT)}$; $V_{(GS)}$ = 10 MΩ; DSG and CHG on; T_A = –40°C to 100°C		8	12	16	V
$V_{(DSGOFF)}$	DSG pin output off voltage	$V_{(DSGOFF)} = V_{(DSG)} - V_{(PACK)}$				0.2	V
$V_{(CHGOFF)}$	CHG pin output off voltage	$V_{(CHGOFF)} = V_{(CHG)} - V_{(BAT)}$				0.2	V
t_r	Rise time	C_L= 4700 pF	$V_{(CHG)}$: $V_{(PACK)} \geq V_{(PACK)}$ + 4 V		400	1000	µs
			$V_{(DSG)}$: $V_{(BAT)} \geq V_{(BAT)}$ + 4 V		400	1000	
t_f	Fall time	C_L= 4700 pF	$V_{(CHG)}$: $V_{(PACK)} + V_{(CHGON)} \geq V_{(PACK)}$+ 1 V		40	200	µs
			$V_{(DSG)}$: VC1 + $V_{(DSGON)} \geq$ VC1 + 1 V		40	200	
$V_{(ZVCHG)}$	ZVCHG clamp voltage	BAT = 4.5 V		3.3	3.5	3.7	V
LOGIC; T_A = –40°C to 100°C (unless otherwise noted)							
$R_{(PULLUP)}$	Internal pullup resistance	$\overline{ALERT}$		60	100	200	kΩ
		$\overline{RESET}$		1	3	6	
V_{OL}	Logic low output voltage level	$\overline{ALERT}$				0.2	V
		$\overline{RESET}$; $V_{(BAT)}$ = 7 V; $V_{(REG25)}$ = 1.5 V; $I_{\overline{(RESET)}}$ = 200 µA				0.4	
		GPOD; $I_{(GPOD)}$ = 50 µA				0.6	
LOGIC SMBC, SMBD, $\overline{PFIN}$, $\overline{PRES}$, SAFE, ALERT, $\overline{DISP}$							
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{OH}	Output voltage high (RC[0:7] bus)	I_L = –0.5 mA		V_{REG25}–0.5			V
V_{OL}	Low-level output voltage	$\overline{PRES}$, $\overline{PFIN}$, $\overline{ALERT}$, $\overline{DISP}$; I_L = 7 mA;				0.4	V
C_I	Input capacitance				5		pF
$I_{(SAFE)}$	SAFE source currents	SAFE active, SAFE = $V_{(REG25)}$ –0.6 V		–3			mA
$I_{lkg(SAFE)}$	SAFE leakage current	SAFE inactive		–0.2		0.2	µA
I_{lkg}	Input leakage current					1	µA
ADC (Unless otherwise specified, the specification limits are valid at all measurement speed modes.)							
	Input voltage range	TS1, TS2, using Internal V_{ref}		–0.2		1	V
	Conversion time				31.5		ms
	Resolution (no missing codes)			16			bits
	Effective resolution			14	15		bits
	Integral nonlinearity					±0.03	%FSR(1)
	Offset error(2)				140	250	µV
	Offset error drift(2)	T_A = 25°C to 85°C			2.5	18	µV/°C
	Full-scale error(3)				±0.1%	±0.7%	
	Full-scale error drift				50		PPM/°C
	Effective input resistance(4)			8			MΩ
COULOMB COUNTER							
	Input voltage range			–0.20		0.20	V
	Conversion time	Single conversion			250		ms
	Effective resolution	Single conversion		15			bits
	Integral nonlinearity	–0.1 V to 0.2 V			±0.007	±0.034	%FSR
		–0.2 V to –0.1 V			±0.007		
	Offset error (5)	T_A = 25°C to 85°C			10		µV

(1) Full-scale reference
(2) Post-calibration performance and no I/O changes during conversion with SRN as the ground reference.
(3) Uncalibrated performance. This gain error can be eliminated with external calibration.
(4) The A/D input is a switched-capacitor input. Because the input is switched, the effective input resistance is a measure of the average resistance.
(5) Post-calibration performance

Electrical Characteristics (continued)

Over operating free-air temperature range, T_A = –40°C to 85°C, $V_{(REG25)}$ = 2.41 V to 2.59 V, $V_{(BAT)}$ = 14 V, $C_{(REG25)}$ = 1 µF, $C_{(REG33)}$ = 2.2 µF; typical values at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Offset error drift			0.4	0.7	µV/°C
	Full-scale error(6) (7)			±0.35%		
	Full-scale error drift			150		PPM/°C
	Effective input resistance(8)	T_A = 25°C to 85°C	2.5			MΩ
INTERNAL TEMPERATURE SENSOR						
$V_{(TEMP)}$	Temperature sensor voltage(9)			–2		mV/°C
VOLTAGE REFERENCE						
	Output voltage		1.215	1.225	1.230	V
	Output voltage drift			65		PPM/°C
HIGH-FREQUENCY OSCILLATOR						
$f_{(OSC)}$	Operating frequency			4.194		MHz
$f_{(EIO)}$	Frequency error (10) (11)		–3%	0.25%	3%	
		T_A = 20°C to 70°C	–2%	0.25%	2%	
$t_{(SXO)}$	Start-up time(12)			2.5	5	ms
LOW-FREQUENCY OSCILLATOR						
$f_{(LOSC)}$	Operating frequency			32.768		kHz
$f_{(LEIO)}$	Frequency error(11) (13)		–2.5%	0.25%	2.5%	
		T_A = 20°C to 70°C	–1.5%	0.25%	1.5%	
$t_{(LSXO)}$	Start-up time(12)				500	µs

(6) Reference voltage for the coulomb counter is typically V_{ref}/3.969 at $V_{(REG25)}$ = 2.5 V, T_A = 25°C.
(7) Uncalibrated performance. This gain error can be eliminated with external calibration.
(8) The CC input is a switched capacitor input. Because the input is switched, the effective input resistance is a measure of the average resistance.
(9) –53.7 LSB/°C
(10) The frequency error is measured from 4.194 MHz.
(11) The frequency drift is included and measured from the trimmed frequency at $V_{(REG25)}$ = 2.5 V, T_A = 25°C.
(12) The start-up time is defined as the time it takes for the oscillator output frequency to be ±3%.
(13) The frequency error is measured from 32.768 kHz.

6.6 Power-on Reset

Over operating free-air temperature range (unless otherwise noted), T_A = –40°C to 85°C, $V_{(REG25)}$ = 2.41 V to 2.59 V, $V_{(BAT)}$ = 14 V, $C_{(REG25)}$ = 1 µF, $C_{(REG33)}$ = 2.2 µF; typical values at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIT–	Negative-going voltage input		1.7	1.8	1.9	V
VHYS	Power-on reset hysteresis		5	125	200	mV
t_{RST}	$\overline{RESET}$ active low time	Active low time after power up or watchdog reset	100	250	560	µs

6.7 Data Flash Characteristics Over Recommended Operating Temperature and Supply Voltage

Typical values at T_A = 25°C and $V_{(REG25)}$ = 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Data retention	See (1)	10			Years
	Flash programming write-cycles		20k			Cycles
$t_{(ROWPROG)}$	Row programming time				2	ms
$t_{(MASSERASE)}$	Mass-erase time				200	ms
$t_{(PAGEERASE)}$	Page-erase time				20	ms
$I_{(DDPROG)}$	Flash-write supply current			5	10	mA
$I_{(DDERASE)}$	Flash-erase supply current			5	10	mA
RAM/REGISTER BACKUP						
$I_{(RB)}$	RB data-retention input current	$V_{(RBI)} > V_{(RBI)MIN}$, $V_{REG25} < V_{IT-}$, T_A = 85°C		1000	2500	nA
		$V_{(RBI)} > V_{(RBI)MIN}$, $V_{REG25} < V_{IT-}$, T_A = 25°C		90	220	
$V_{(RB)}$	RB data-retention input voltage (1)		1.7			V

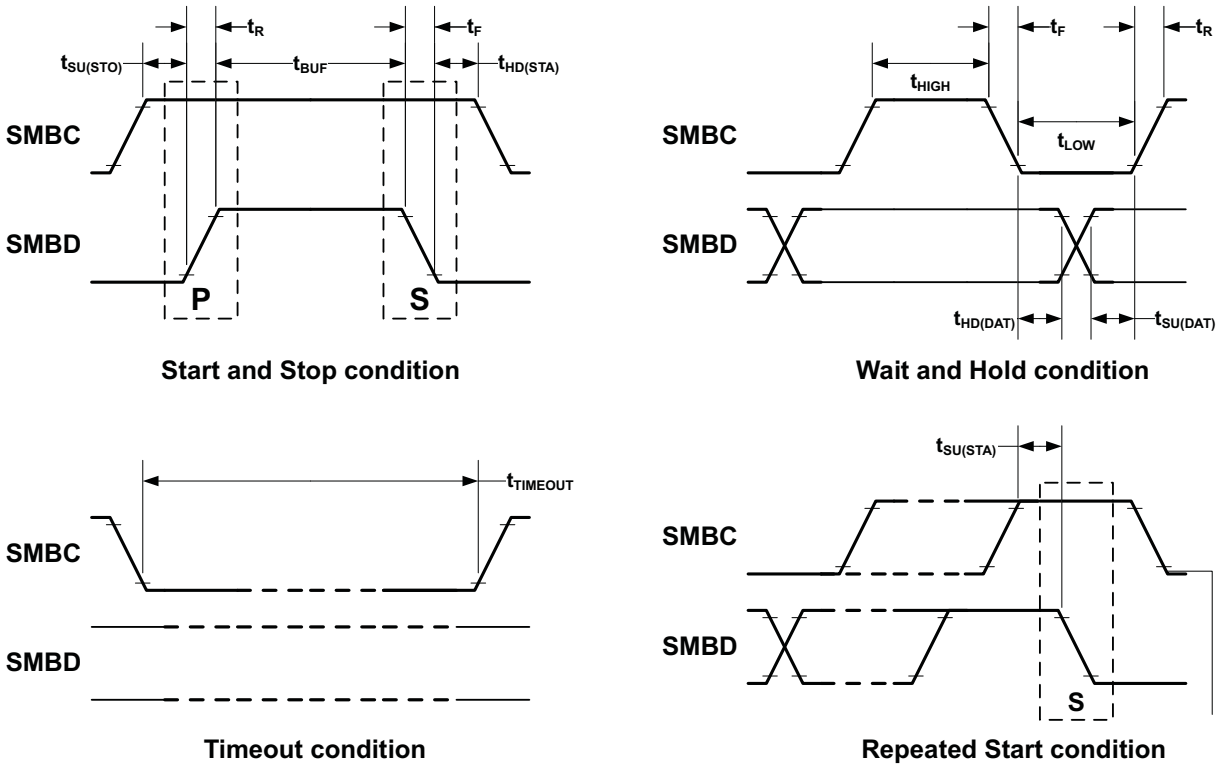
(1) Specified by design. Not production tested.

6.8 SMBus Timing Requirements

T_A = –40°C to 85°C Typical Values at T_A = 25°C and V_{REG25} = 2.5 V (Unless Otherwise Noted)

			MIN	NOM	MAX	UNIT
$f_{(SMB)}$	SMBus operating frequency	Slave mode, SMBC 50% duty cycle	10		100	kHz
$f_{(MAS)}$	SMBus master clock frequency	Master mode, No clock low slave extend		51.2		kHz
$t_{(BUF)}$	Bus free time between start and stop (see Figure 1)		4.7			µs
$t_{(HD:STA)}$	Hold time after (repeated) start (see Figure 1)		4			µs
$t_{(SU:STA)}$	Repeated start setup time (see Figure 1)		4.7			µs
$t_{(SU:STO)}$	Stop setup time (see Figure 1)		4			µs
$t_{(HD:DAT)}$	Data hold time (see Figure 1)	Receive mode	0			ns
		Transmit mode	300			
$t_{(SU:DAT)}$	Data setup time (see Figure 1)		250			ns
$t_{(TIMEOUT)}$	Error signal/detect (see Figure 1)	See (1)	25		35	µs
$t_{(LOW)}$	Clock low period (see Figure 1)		4.7			µs
$t_{(HIGH)}$	Clock high period (see Figure 1)	See (2)	4		50	µs
$t_{(LOW:SEXT)}$	Cumulative clock low slave extend time	See (3)			25	ms
$t_{(LOW:MEXT)}$	Cumulative clock low master extend time (see Figure 1)	See (4)			10	ms
t_f	Clock/data fall time	See (5)			300	ns
t_r	Clock/data rise time	See (6)			1000	ns

(1) The bq20z655-R1 times out when any clock low exceeds $t_{(TIMEOUT)}$.
(2) $t_{(HIGH)}$, Max, is the minimum bus idle time. SMBC = SMBD = 1 for t > 50 ms causes reset of any transaction involving bq20z655-R1 that is in progress. This specification is valid when the NC_SMB control bit remains in the default cleared state (CLK[0]=0).
(3) $t_{(LOW:SEXT)}$ is the cumulative time a slave device is allowed to extend the clock cycles in one message from initial start to the stop.
(4) $t_{(LOW:MEXT)}$ is the cumulative time a master device is allowed to extend the clock cycles in one message from initial start to the stop.
(5) Rise time t_r = VILMAX – 0.15) to (VIHMIN + 0.15)
(6) Fall time t_f = 0.9 V_{DD} to (VILMAX – 0.15)



A. SCLKACK is the acknowledge-related clock pulse generated by the master.

Figure 1. SMBus Timing Diagram

6.9 Typical Characteristics

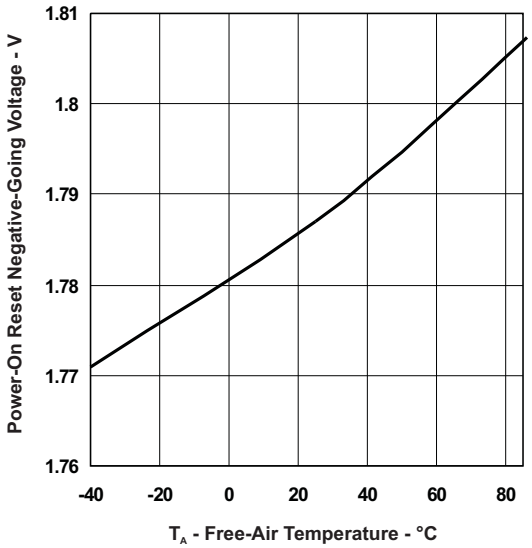


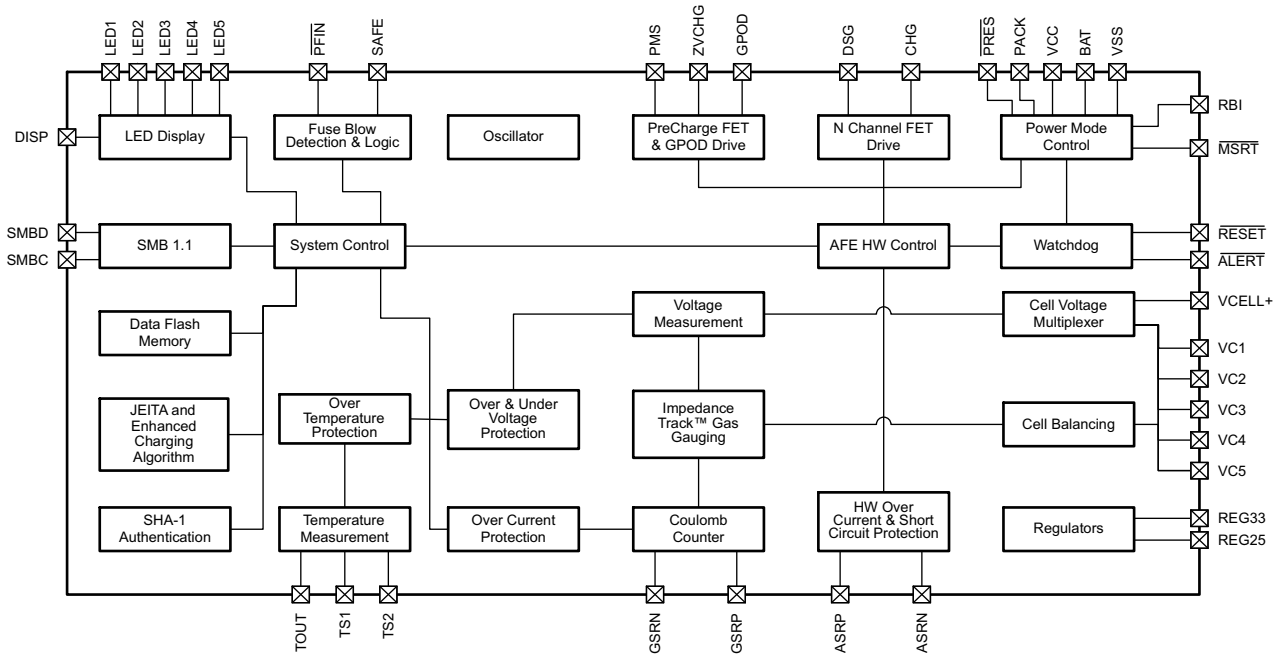
Figure 2. Power On Reset Behavior vs Free-Air Temperature

7 Detailed Description

7.1 Overview

The bq20z655-R1 incorporating patented Impedance Track™ technology is a single IC solution designed for battery-pack or in-system installation. This SBS-compliant gas gauge and protection IC implemented with Impedance Track™ gas gauging technology continuously analyzes the battery impedance, resulting in superior gas-gauging accuracy.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Feature Set

7.3.1.1 Primary (1st Level) Safety Features

The bq20z655-R1 supports a wide range of battery and system protection features that can easily be configured. The primary safety features include:

- Cell over/undervoltage protection
- Charge and discharge overcurrent
- Short Circuit protection
- Charge and discharge overtemperature with independent alarms and thresholds for each thermistor
- AFE Watchdog

7.3.1.2 Secondary (2nd Level) Safety Features

The secondary safety features of the bq20z655-R1 can be used to indicate more serious faults through the SAFE pin. This pin can be used to blow an in-line fuse to permanently disable the battery pack from charging or discharging. The secondary safety protection features include:

- Safety overvoltage
- Safety undervoltage
- 2nd level protection IC input
- Safety overcurrent in charge and discharge

Feature Description (continued)

- Safety over-temperature in charge and discharge with independent alarms and thresholds for each thermistor
- Charge FET and zero-volt charge FET fault
- Discharge FET fault
- Cell imbalance detection (active and at rest)
- Open thermistor detection
- Fuse blow detection
- AFE communication fault

7.3.1.3 Charge Control Features

The bq20z655-R1 charge control features include:

- Supports JEITA temperature ranges. Reports charging voltage and charging current according to the active temperature range.
- Handles more complex charging profiles. Allows for splitting the standard temperature range into two sub-ranges and allows for varying the charging current according to the cell voltage.
- Reports the appropriate charging current needed for constant current charging and the appropriate charging voltage needed for constant voltage charging to a smart charger using SMBus broadcasts.
- Determines the chemical state of charge of each battery cell using Impedance Track™ and can reduce the charge difference of the battery cells in fully charged state of the battery pack gradually using cell balancing algorithm during charging. This prevents fully charged cells from overcharging and causing excessive degradation and also increases the usable pack energy by preventing premature charge termination
- Supports pre-charging and zero-volt charging
- Supports charge inhibit and charge suspend if battery pack temperature is out of temperature range
- Reports charging fault and also indicate charge status through charge and discharge alarms.

7.3.1.4 Gas Gauging

The bq20z655-R1 uses the Impedance Track™ Technology to measure and calculate the available charge in battery cells. The achievable accuracy is better than 1% error over the lifetime of the battery and there is no full charge discharge learning cycle required.

See the *Theory and Implementation of Impedance Track Battery Fuel-Gauging Algorithm* application note (SLUA364) for further details.

7.3.1.5 Lifetime Data Logging Features

The bq20z655-R1 offers lifetime data logging, where important measurements are stored for warranty and analysis purposes. The data monitored include:

- Lifetime maximum temperature
- Lifetime maximum temperature count
- Lifetime maximum temperature duration
- Lifetime minimum temperature
- Lifetime maximum battery cell voltage
- Lifetime maximum battery cell voltage count
- Lifetime maximum battery cell voltage duration
- Lifetime minimum battery cell voltage
- Lifetime maximum battery pack voltage
- Lifetime minimum battery pack voltage
- Lifetime maximum charge current
- Lifetime maximum discharge current
- Lifetime maximum charge power
- Lifetime maximum discharge power
- Lifetime maximum average discharge current
- Lifetime maximum average discharge power

Feature Description (continued)

- Lifetime average temperature

7.3.1.6 Authentication

The bq20z655-R1 supports authentication by the host using SHA-1.

7.3.2 Battery Parameter Measurements

The bq20z655-R1 uses an integrating delta-sigma analog-to-digital converter (ADC) for current measurement, and a second delta-sigma ADC for individual cell and battery voltage, and temperature measurement.

7.3.2.1 Charge and Discharge Counting

The integrating delta-sigma ADC measures the charge/discharge flow of the battery by measuring the voltage drop across a small-value sense resistor between the SR1 and SR2 pins. The integrating ADC measures bipolar signals from –0.25 V to 0.25 V. The bq20z655-R1 detects charge activity when $V_{SR} = V_{(SRP)}-V_{(SRN)}$is positive and discharge activity when $V_{SR} = V_{(SRP)} - V_{(SRN)}$ is negative. The bq20z655-R1 continuously integrates the signal over time, using an internal counter. The fundamental rate of the counter is 0.65 nVh.

7.3.2.2 Voltage

The bq20z655-R1 updates the individual series cell voltages at one second intervals. The internal ADC of the bq20z655-R1 measures the voltage, scales and calibrates it appropriately. This data is also used to calculate the impedance of the cell for the Impedance Track™ gas-gauging.

7.3.2.3 Current

The bq20z655-R1 uses the SRP and SRN inputs to measure and calculate the battery charge and discharge current using a 5-mΩ to 20-mΩ typical sense resistor.

7.3.2.4 Wake Function

The bq20z655-R1 can exit sleep mode, if enabled, by the presence of a programmable level of current signal across SRP and SRN.

7.3.2.5 Auto Calibration

The bq20z655-R1 provides an auto-calibration feature to cancel the voltage offset error across SRN and SRP for maximum charge measurement accuracy. The bq20z655-R1 performs auto-calibration when the SMBus lines stay low continuously for a minimum of a programmable amount of time.

7.3.2.6 Temperature

The bq20z655-R1 has an internal temperature sensor and 2 external temperature sensor inputs, TS1 and TS2, used in conjunction with two identical NTC thermistors (default are Semitec 103AT) to sense the battery environmental temperature. The bq20z655-R1 can be configured to use the internal temperature sensor or up to 2 external temperature sensors.

7.4 Device Functional Modes

7.4.1 Power Modes

The bq20z655-R1 supports three different power modes to reduce power consumption:

- In Normal Mode, the bq20z655-R1 performs measurements, calculations, protection decisions and data updates in 1 second intervals. Between these intervals, the bq20z655-R1 is in a reduced power stage.
- In Sleep Mode, the bq20z655-R1 performs measurements, calculations, protection decisions and data update in adjustable time intervals. Between these intervals, the bq20z655-R1 is in a reduced power stage. The bq20z655-R1 has a wake function that enables exit from Sleep mode, when current flow or failure is detected.
- In Shutdown Mode, the bq20z655-R1 is completely disabled.

7.5 Programming

7.5.1 Configuration

7.5.1.1 Oscillator Function

The bq20z655-R1 fully integrates the system oscillators therefore, no external components are required for this feature.

7.5.1.2 System Present Operation

The bq20z655-R1 periodically verifies the $\overline{\text{PRES}}$ pin and detects that the battery is present in the system through a low state on a $\overline{\text{PRES}}$ input. When this occurs, the bq20z655-R1 enters normal operating mode. When the pack is removed from the system and the $\overline{\text{PRES}}$ input is high, the bq20z655-R1 enters the battery-removed state, disabling the charge, discharge, and ZVCHG FETs. The $\overline{\text{PRES}}$ input is ignored and can be left floating when non-removal mode is set in the data flash.

7.5.2 Communications

The bq20z655-R1 uses SMBus v1.1 with Master Mode and package error checking (PEC) options per the SBS specification.

7.5.2.1 SMBus On and Off State

The bq20z655-R1 detects an SMBus off state when SMBC and SMBD are logic-low for ≥ 2 seconds. Clearing this state requires either SMBC or SMBD to transition high. Within 1 ms, the communication bus is available.

Programming (continued)

7.5.3 SBS Commands

Table 1. SBS Commands

SBS CMD	MODE	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
0x00	R/W	ManufacturerAccess	Hex	2	0x0000	0xffff	—	—
0x01	R/W	RemainingCapacityAlarm	Integer	2	0	700 or 1000	300 or 432	mAh or 10 mWh
0x02	R/W	RemainingTimeAlarm	Unsigned integer	2	0	30	10	min
0x03	R/W	BatteryMode	Hex	2	0x0000	0xffff	—	—
0x04	R/W	AtRate	Integer	2	–32,768	32,767	—	mA or 10 mW
0x05	R	AtRateTimeToFull	Unsigned integer	2	0	65,535	—	min
0x06	R	AtRateTimeToEmpty	Unsigned integer	2	0	65,535	—	min
0x07	R	AtRateOK	Unsigned integer	2	0	65,535	—	—
0x08	R	Temperature	Unsigned integer	2	0	65,535	—	0.1°K
0x09	R	Voltage	Unsigned integer	2	0	20,000	—	mV
0x0a	R	Current	Integer	2	–32,768	32767	—	mA
0x0b	R	AverageCurrent	Integer	2	–32,768	32,767	—	mA
0x0c	R	MaxError	Unsigned integer	1	0	100	—	%
0x0d	R	RelativeStateOfCharge	Unsigned integer	1	0	100	—	%
0x0e	R	AbsoluteStateOfCharge	Unsigned integer	1	0	100+	—	%
0x0f	R/W	RemainingCapacity	Unsigned integer	2	0	65,535	—	mAh or 10 mWh
0x10	R	FullChargeCapacity	Unsigned integer	2	0	65,535	—	mAh or 10 mWh
0x11	R	RunTimeToEmpty	Unsigned integer	2	0	65,534	—	min
0x12	R	AverageTimeToEmpty	Unsigned integer	2	0	65,534	—	min
0x13	R	AverageTimeToFull	Unsigned integer	2	0	65,534	—	min
0x14	R	ChargingCurrent	Unsigned integer	2	0	65,534	—	mA
0x15	R	ChargingVoltage	Unsigned integer	2	0	65,534	—	mV
0x16	R	BatteryStatus	Hex	2	0x0000	0xdbff	—	—
0x17	R/W	CycleCount	Unsigned integer	2	0	65,535	0	—
0x18	R/W	DesignCapacity	Integer	2	0	32,767	4400 or 6336	mAh or 10 mWh
0x19	R/W	DesignVoltage	Integer	2	7000	18,000	14,400	mV
0x1a	R/W	SpecificationInfo	Hex	2	0x0000	0xffff	0x0031	—
0x1b	R/W	ManufactureDate	Unsigned integer	2	0	65,535	0	—
0x1c	R/W	SerialNumber	Hex	2	0x0000	0xffff	0x0000	—
0x20	R/W	ManufacturerName	String	20+1	—	—	Texas Instruments	—

Programming (continued)

Table 1. SBS Commands (continued)

SBS CMD	MODE	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
0x21	R/W	DeviceName	String	20+1	—	—	bq20z655-R1	—
0x22	R/W	DeviceChemistry	String	4+1	—	—	LION	—
0x23	R	ManufacturerData	String	14+1	—	—	—	—
0x2f	R/W	Authenticate	String	20+1	—	—	—	—
0x3c	R	CellVoltage4	Unsigned integer	2	0	65,535	—	mV
0x3d	R	CellVoltage3	Unsigned integer	2	0	65,535	—	mV
0x3e	R	CellVoltage2	Unsigned integer	2	0	65,535	—	mV
0x3f	R	CellVoltage1	Unsigned integer	2	0	65,535	—	mV

Table 2. Extended SBS Commands

SBS CMD	MODE	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
0x45	R	AFEData	String	11+1	—	—	—	—
0x46	R/W	FETControl	Hex	2	0x00	0xff	—	—
0x4f	R	StateOfHealth	Hex	2	0x0000	0xffff	—	%
0x51	R	SafetyStatus	Hex	2	0x0000	0xffff	—	—
0x52	R	PFAlert	Hex	2	0x0000	0xffff	—	—
0x53	R	PFStatus	Hex	2	0x0000	0xffff	—	—
0x54	R	OperationStatus	Hex	2	0x0000	0xffff	—	—
0x55	R	ChargingStatus	Hex	2	0x0000	0xffff	—	—
0x57	R	ResetData	Hex	2	0x0000	0xffff	—	—
0x58	R	WDResetData	Unsigned integer	2	0	65,535	—	—
0x5a	R	PackVoltage	Unsigned integer	2	0	65,535	—	mV
0x5d	R	AverageVoltage	Unsigned integer	2	0	65,535	—	mV
0x5e	R	TS1Temperature	Integer	2	-400	1200	—	0.1°C
0x5f	R	TS2Temperature	Integer	2	-400	1200	—	0.1°C
0x60	R/W	UnSealKey	Hex	4	0x00000000	0xffffffff	—	—
0x61	R/W	FullAccessKey	Hex	4	0x00000000	0xffffffff	—	—
0x62	R/W	PFKey	Hex	4	0x00000000	0xffffffff	—	—
0x63	R/W	AuthenKey3	Hex	4	0x00000000	0xffffffff	—	—
0x64	R/W	AuthenKey2	Hex	4	0x00000000	0xffffffff	—	—
0x65	R/W	AuthenKey1	Hex	4	0x00000000	0xffffffff	—	—
0x66	R/W	AuthenKey0	Hex	4	0x00000000	0xffffffff	—	—
0x68	R	SafetyAlert2	Hex	2	0x0000	0x000f	—	—
0x69	R	SafetyStatus2	Hex	2	0x0000	0x000f	—	—
0x6a	R	PFAlert2	Hex	2	0x0000	0x000f	—	—
0x6b	R	PFStatus2	Hex	2	0x0000	0x000f	—	—
0x6c	R	ManufBlock1	String	20	—	—	—	—
0x6d	R	ManufBlock2	String	20	—	—	—	—
0x6e	R	ManufBlock3	String	20	—	—	—	—

Table 2. Extended SBS Commands (continued)

SBS CMD	MODE	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
0x6f	R	ManufBlock4	String	20	—	—	—	—
0x70	R/W	ManufacturerInfo	String	31+1	—	—	—	—
0x71	R/W	SenseResistor	Unsigned integer	2	0	65,535	—	μΩ
0x72	R	TempRange	Hex	2	—	—	—	—
0x73	R	LifetimeData1	String	32+1	—	—	—	—
0x74	R	LifetimeData2	String	8+1	—	—	—	—
0x77	R/W	DataFlashSubClassID	Hex	2	0x0000	0xffff	—	—
0x78	R/W	DataFlashSubClassPage1	Hex	32	—	—	—	—
0x79	R/W	DataFlashSubClassPage2	Hex	32	—	—	—	—
0x7a	R/W	DataFlashSubClassPage3	Hex	32	—	—	—	—
0x7b	R/W	DataFlashSubClassPage4	Hex	32	—	—	—	—
0x7c	R/W	DataFlashSubClassPage5	Hex	32	—	—	—	—
0x7d	R/W	DataFlashSubClassPage6	Hex	32	—	—	—	—
0x7e	R/W	DataFlashSubClassPage7	Hex	32	—	—	—	—
0x7f	R/W	DataFlashSubClassPage8	Hex	32	—	—	—	—

8 Application and Implementation

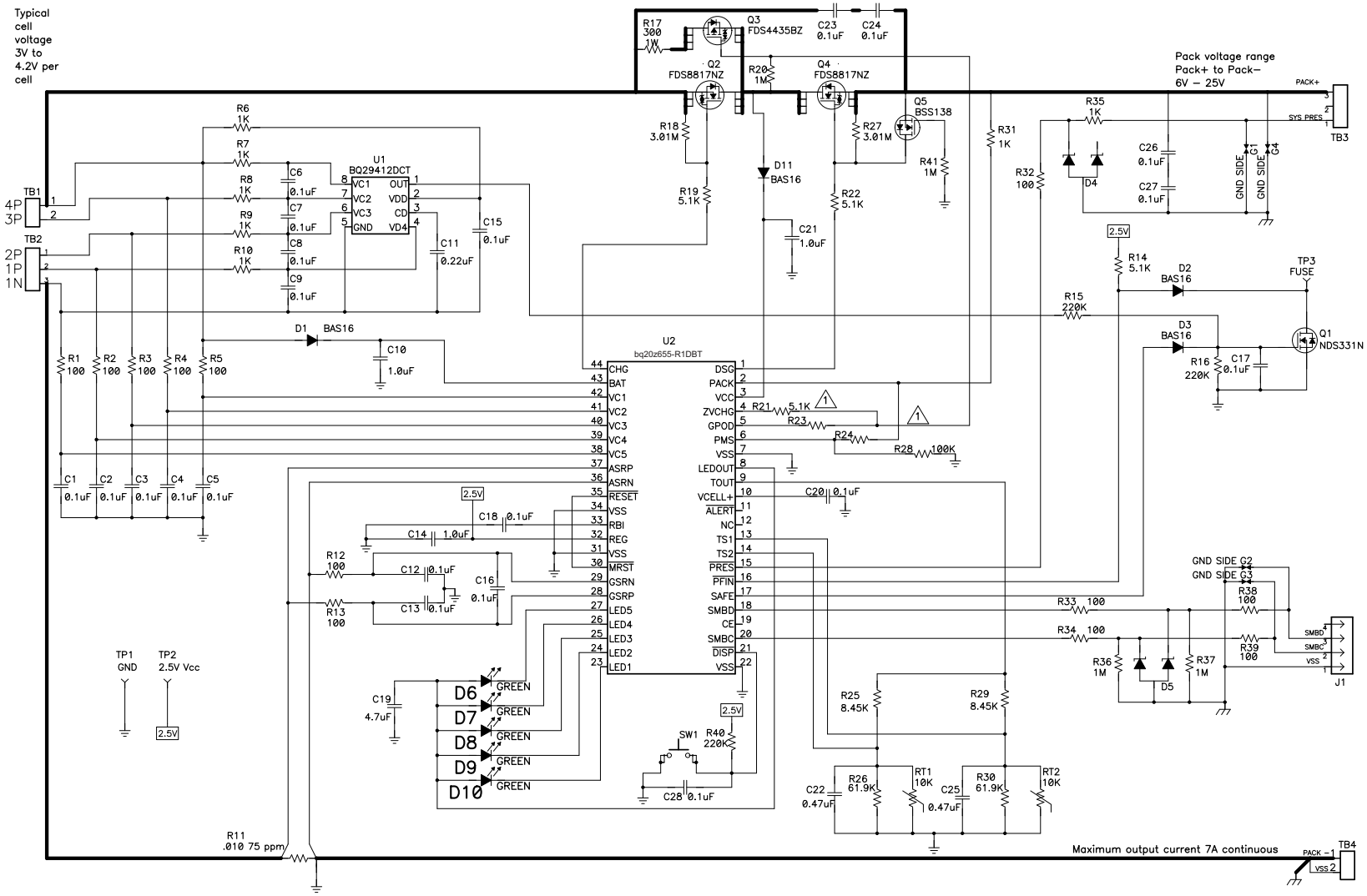
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The bq20z655-R1 is a gas gauge with primary protection support, and that can be used with a 2-series to 4-series Li-Ion/Li Polymer battery pack. To implement and design a comprehensive set of parameters for a specific battery pack, users need the BQEV graphical user-interface tool installed on a PC during development. The firmware installed on the BQEV tool has default values for this product, which are summarized in the bq20z655 Technical Reference Manual (SLUU493). Using the tool, BQEV these default values can be changed to cater to specific application requirements during development once the system parameters, such as fault trigger thresholds for protection, enable/disable of certain features for operation, configuration of cells, chemistry that best matches the cell used, and more are known. This data is referred to as the *golden image*.

8.2 Typical Application



Install these parts for various pre–charge options. See bq20z65 EVM user guide.
Default configuration has R23 & R24 NOT installed.

Figure 3. Application Schematic

8.2.1 Design Requirements

Table 3 shows the default settings for the main parameters. Use the BQEV tool to update the settings to meet the specific application or battery pack configuration requirements.

Table 3. Design Parameters

PARAMETER	EXAMPLE VALUE
Cell configuration	4s1p (4 series with 1 parallel)
Design capacity	4400 mAH
Device chemistry	0100 (LION)
Cell overvoltage at standard temperature	4300 mV
Cell undervoltage	2200 mV
Cell Shutdown voltage	1750 mV
Overcurrent in CHARGE mode	6000 mA
Overcurrent in DISCHARGE mode	–6000 mA
Short circuit in CHARGE mode	0.1 V/Rsense across SRP, SRN
Short circuit in DISCHARGE mode	0.1 V/Rsense across SRP, SRN
Safety overvoltage	4500 mV
Cell balancing	Disabled
Internal and external temperature sensor	External temperature sensor is used
Undertemperature charging	0°C
Undertemperature discharging	0°C
BROADCAST mode	Disabled
Battery Trip Point (BTP) with active high interrupt	Disabled

8.2.2 Detailed Design Procedure

8.2.2.1 Choosing the Correct Chemistry

For the Impedance Track™ algorithm to work properly, the exact chemistry of the lithium cells needs to be known and the correct .SENC file needs to be loaded.

If you are using the bqEASY design wizard, it asks you to choose the correct chemistry from a list of manufacturers and model numbers, or test for a compatible chemistry using a 4-point test.

NOTE

Success of the 4-point test is contingent on an accurate voltage calibration.

The process for updating the .SENC file is outlined in detail in the application report Updating Firmware With The bq20zxx and EVM.

8.2.2.2 High-Current Path

The high-current path begins at the PACK+ terminal of the battery pack. As charge current travels through the pack, it finds its way through protection FETs, a chemical fuse, the lithium-ion cells and cell connections, and the sense resistor, and then returns to the PACK– terminal. In addition, some components are placed across the PACK+ and PACK– terminals to reduce effects from electrostatic discharge.

8.2.2.3 Protection FETs

Select the N-channel charge and discharge FETs for a given application. Most portable battery applications are a good match for the CSD17308Q3. The TI CSD17308Q3 is a 47-A, 30-V device with Rds(on) of 8.2 mΩ when the gate drive voltage is 8 V.

If a precharge FET is used, R1 is calculated to limit the precharge current to the desired rate. Be sure to account for the power dissipation of the series resistor. The precharge current is limited to (VCHARGER – VBAT)/R1 and maximum power dissipation is (Vcharger – Vbat)2/R1.

The gates of all protection FETs are pulled to the source with a high-value resistor between the gate and source to ensure they are turned off if the gate drive is open.

Capacitors C1 and C2 help protect the FETs during an ESD event. Using two devices ensures normal operation if one becomes shorted. To have good ESD protection, the copper trace inductance of the capacitor leads must be designed to be as short and wide as possible. Ensure that the voltage rating of both C1 and C2 are adequate to hold off the applied voltage if one of the capacitors becomes shorted.

8.2.2.4 Lithium-Ion Cell Connections

The important part to remember about the cell connections is that high current flows through the top and bottom connections; therefore, the voltage sense leads at these points must be made with a Kelvin connection to avoid any errors due to a drop in the high-current copper trace. The location marked 4P in indicates the Kelvin connection of the most positive battery node.

8.2.2.5 Sense Resistor

As with the cell connections, the quality of the Kelvin connections at the sense resistor is critical. The sense resistor must have a temperature coefficient no greater than 50 ppm to minimize current measurement drift with temperature. Choose the value of the sense resistor to correspond to the available overcurrent and short circuit ranges of the bq20z655. Select the smallest value possible to minimize the negative voltage generated on the VSS nodes during a short circuit.

8.2.2.6 ESD Mitigation

A pair of series 0.1-μF ceramic capacitors is placed across the PACK+ and PACK– terminals to help in the mitigation of external electrostatic discharges. The two devices in series ensure continued operation of the pack if one of the capacitors becomes shorted. Optionally, a tranzorb such as the SMBJ2A can be placed across the terminals to further improve ESD immunity.

8.2.2.7 System Present

The System Present signal is used to inform the gas gauge whether the pack is installed into or removed from the system. In the host system, this pin is grounded. The PRES pin of the bq20z655 is occasionally sampled to test for system present. To save power, an internal pullup is provided by the gas gauge during a brief 4-μs sampling pulse once per second. A resistor can be used to pull the signal low and the resistance must be 20 kΩ or lower to insure that the test pulse is lower than the VIL limit. The pullup current source is typically 10 μA to 20 μA.

Because the System Present signal is part of the pack connector interface to the outside world, it must be protected from external electrostatic discharge events. An integrated ESD protection on the PRES device pin reduces the external protection requirement to just R29 for an 8-kV ESD contact rating. However, if it is possible that the System Present signal may short to PACK+, then a resistor, diode combo must be included for high-voltage protection.

8.2.2.8 SMBus Communication

The SMBus clock and data pins have integrated high-voltage ESD protection circuits, however, adding a Zener diode and series resistor provides more robust ESD performance.

8.2.3 Application Curves

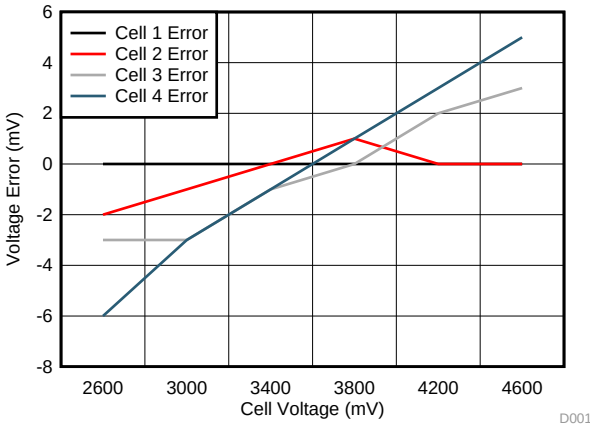


Figure 4. Cell Voltage Error at 25°C

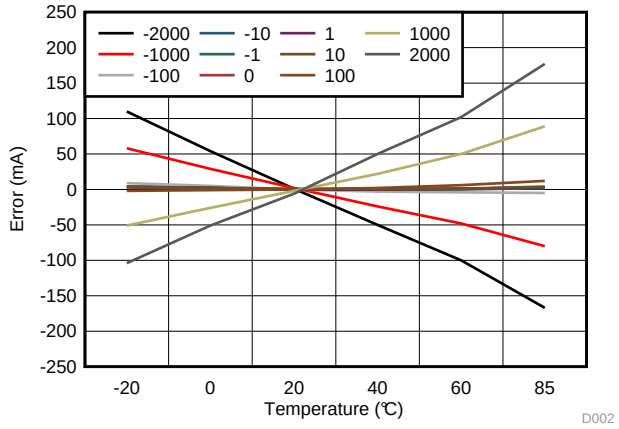


Figure 5. Current vs Temperature

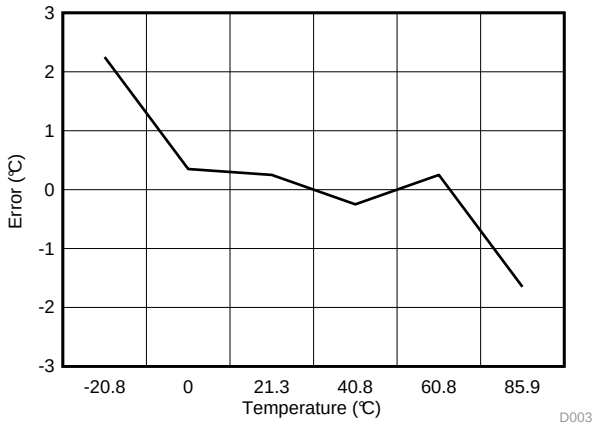


Figure 6. TS1 Error vs Temperature

9 Power Supply Recommendations

The device manages its supply voltage dynamically according to the operation conditions. Normally, the BAT input is the primary power source to the device. The BAT pin should be connected to the positive termination of the battery stack. The input voltage for the BAT pin ranges from 4.5 V to 25 V. The VCC pin is the secondary power input, which activates when the BAT voltage falls below minimum Vcc. This allows the device to source power from a charger (if present) connected to the PACK pin. The VCC pin should be connected to the common drain of the CHG and DSG FETs. The charger input should be connected to the PACK pin.

10 Layout

10.1 Layout Guidelines

A battery fuel gauge circuit board is a challenging environment due to the fundamental incompatibility of high-current traces and ultra-low current semiconductor devices. The best way to protect against unwanted trace-to-trace coupling is with a component placement, such as that shown in Figure 11, where the high-current section is on the opposite side of the board from the electronic devices. Clearly this is not possible in many situations due to mechanical constraints. Still, every attempt should be made to route high-current traces away from signal traces, which enter the directly. IC references and registers can be disturbed and in rare cases damaged due to magnetic and capacitive coupling from the high-current path. During surge current and ESD events, the high-current traces appear inductive and can couple unwanted noise into sensitive nodes of the gas gauge electronics, as illustrated in Figure 12.

Kelvin voltage sensing is extremely important to accurately measure current and top and bottom cell voltages. Place all filter components as close as possible to the device. Route the traces from the sense resistor in parallel to the filter circuit. Adding a ground plane around the filter network can add additional noise immunity. Figure 7 and Figure 8 demonstrates correct kelvin current sensing.

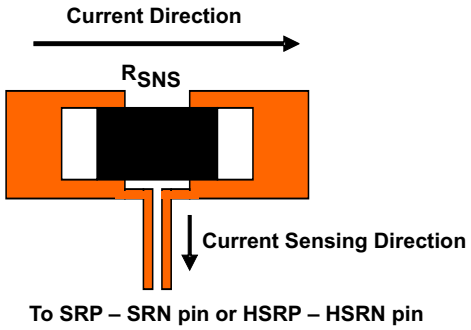


Figure 7. Sensing Resistor PCB Layout

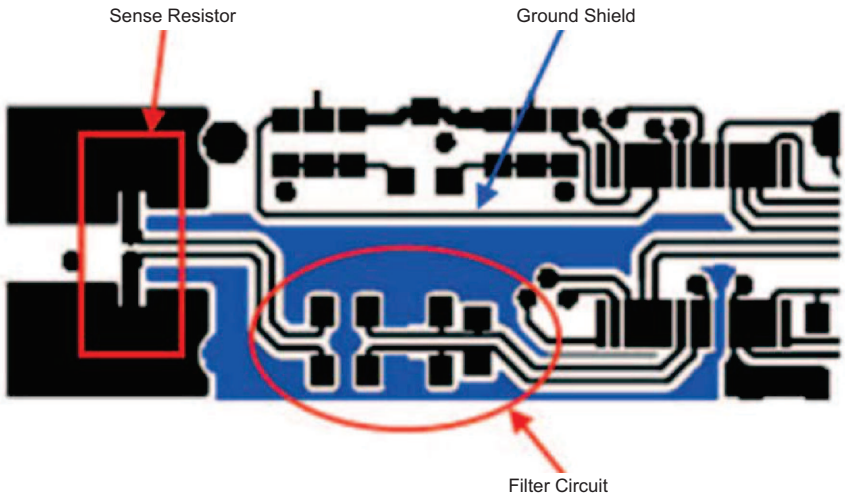


Figure 8. Sense Resistor, Ground Shield, and Filter Circuit Layout

10.1.1 Protector FET Bypass and Pack Terminal Bypass Capacitors

The general principle is to use wide copper traces to lower the inductance of the bypass capacitor circuit. In Figure 9, an example layout demonstrates this technique.

Layout Guidelines (continued)

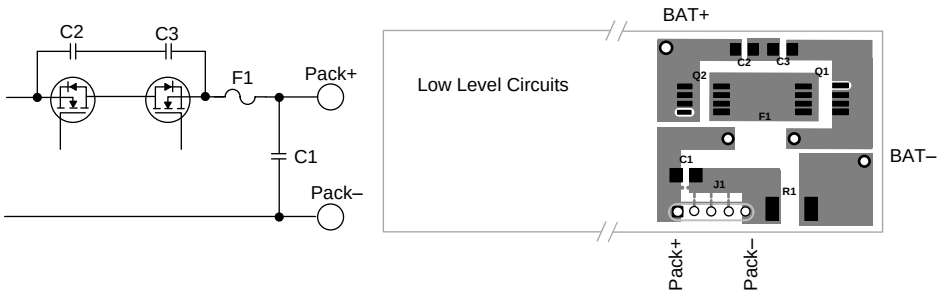


Figure 9. Use Wide Copper Traces to Lower the Inductance of Bypass Capacitors C1, C2, and C3

10.1.2 ESD Spark Gap

Protect SMBus Clock, Data, and other communication lines from ESD with a spark gap at the connector. The pattern in Figure 10 recommended, with 0.2-mm spacing between the points.

Figure 10. Recommended Spark-Gap Pattern Helps Protect Communication Lines from ESD

10.2 Layout Example

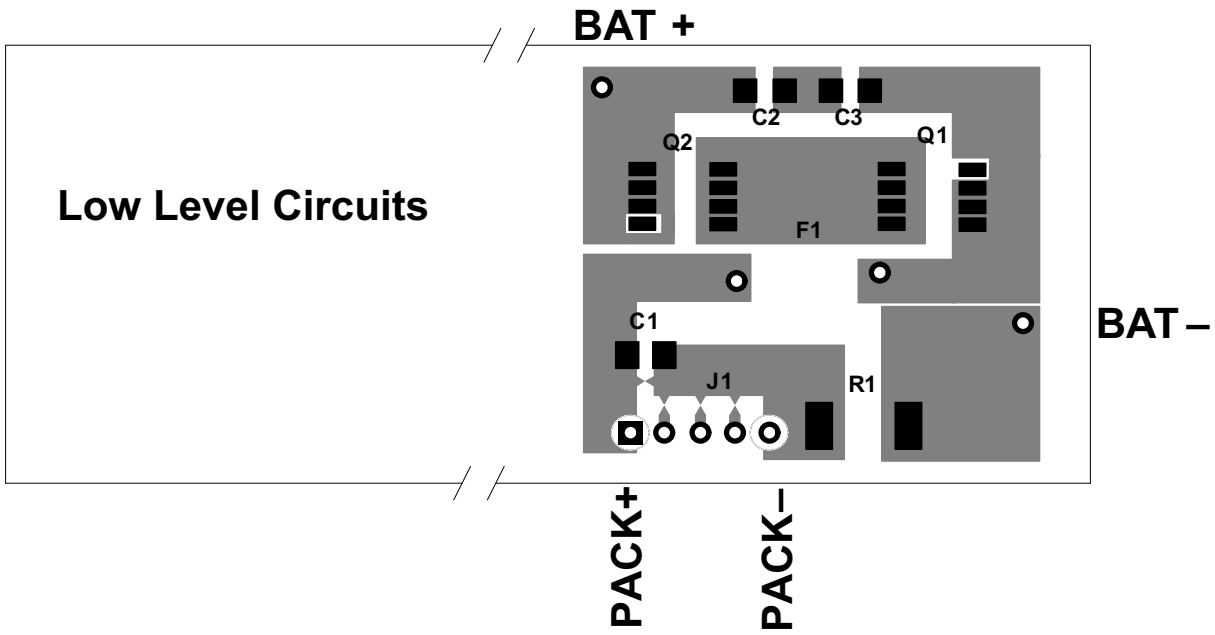


Figure 11. Separating High- and Low-Current Sections Provides an Advantage in Noise Immunity

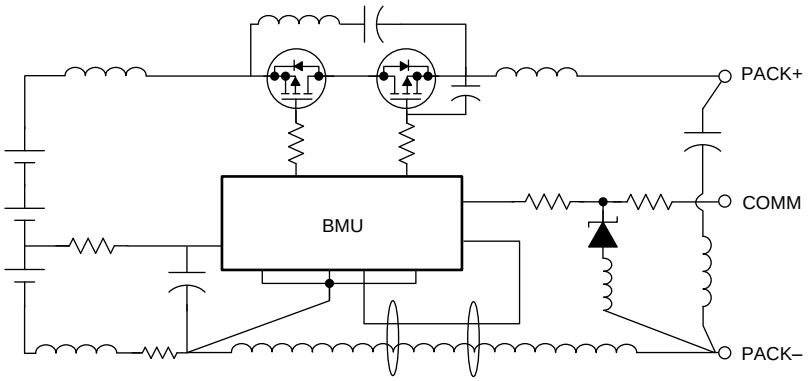


Figure 12. Avoid Close Spacing Between High-Current and Low-Level Signal Lines

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *bq20z655 Technical Reference*, SLUU493
- *bq20z655EVM and bq34z651EVM SBS 1.1 Impedance Track Technology-Enabled Evaluation Module*, SLUU697
- *Quick-Start Guide for bq20zxx Family Gas Gauges*, SLUA421

For additional application notes related to the bq20zXX family see the bq20z80 page on www.ti.com.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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11.3 Trademarks

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11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ20Z655DBT-R1	ACTIVE	TSSOP	DBT	44	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-250C-1 YEAR	-40 to 85	BQ20Z655	Samples
BQ20Z655DBTR-R1	ACTIVE	TSSOP	DBT	44	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ20Z655	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

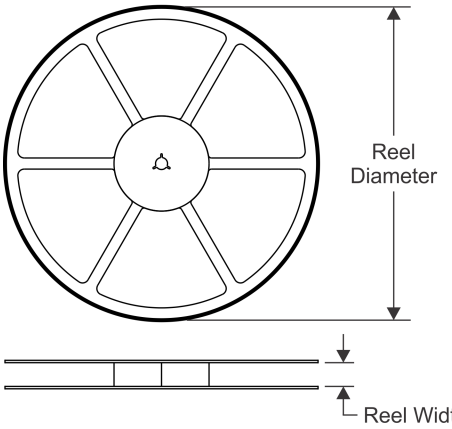
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

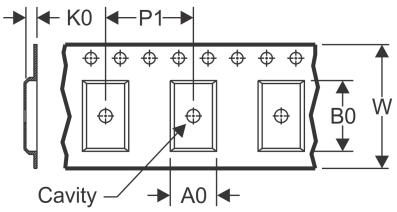
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

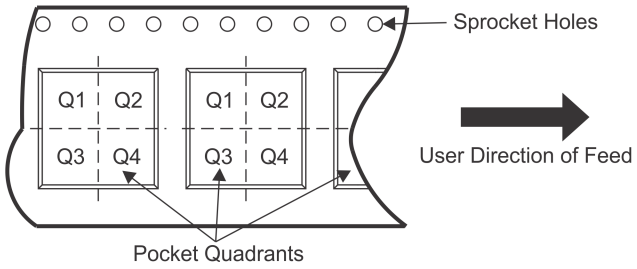


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

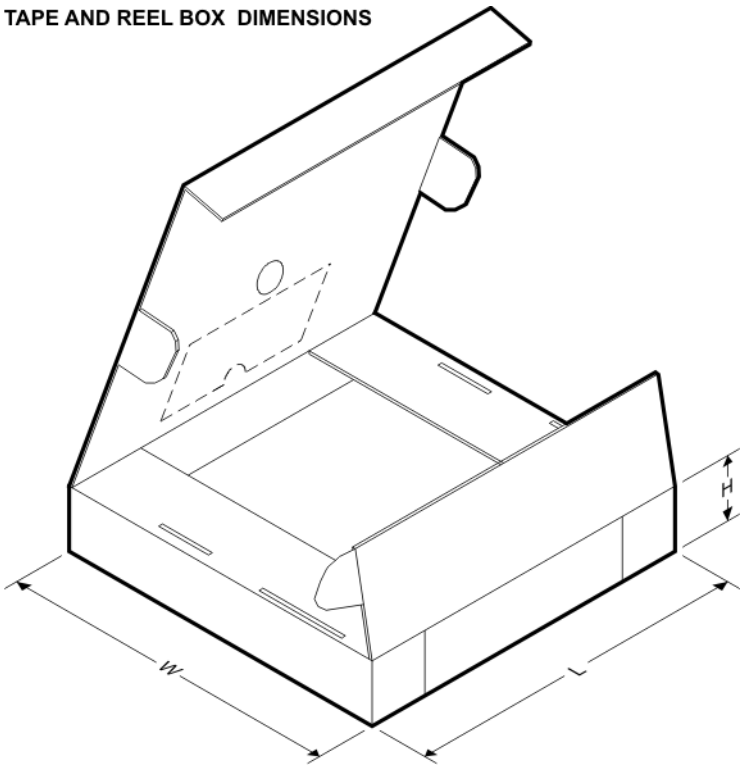
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ20Z655DBTR-R1	TSSOP	DBT	44	2000	330.0	24.4	6.8	11.7	1.6	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

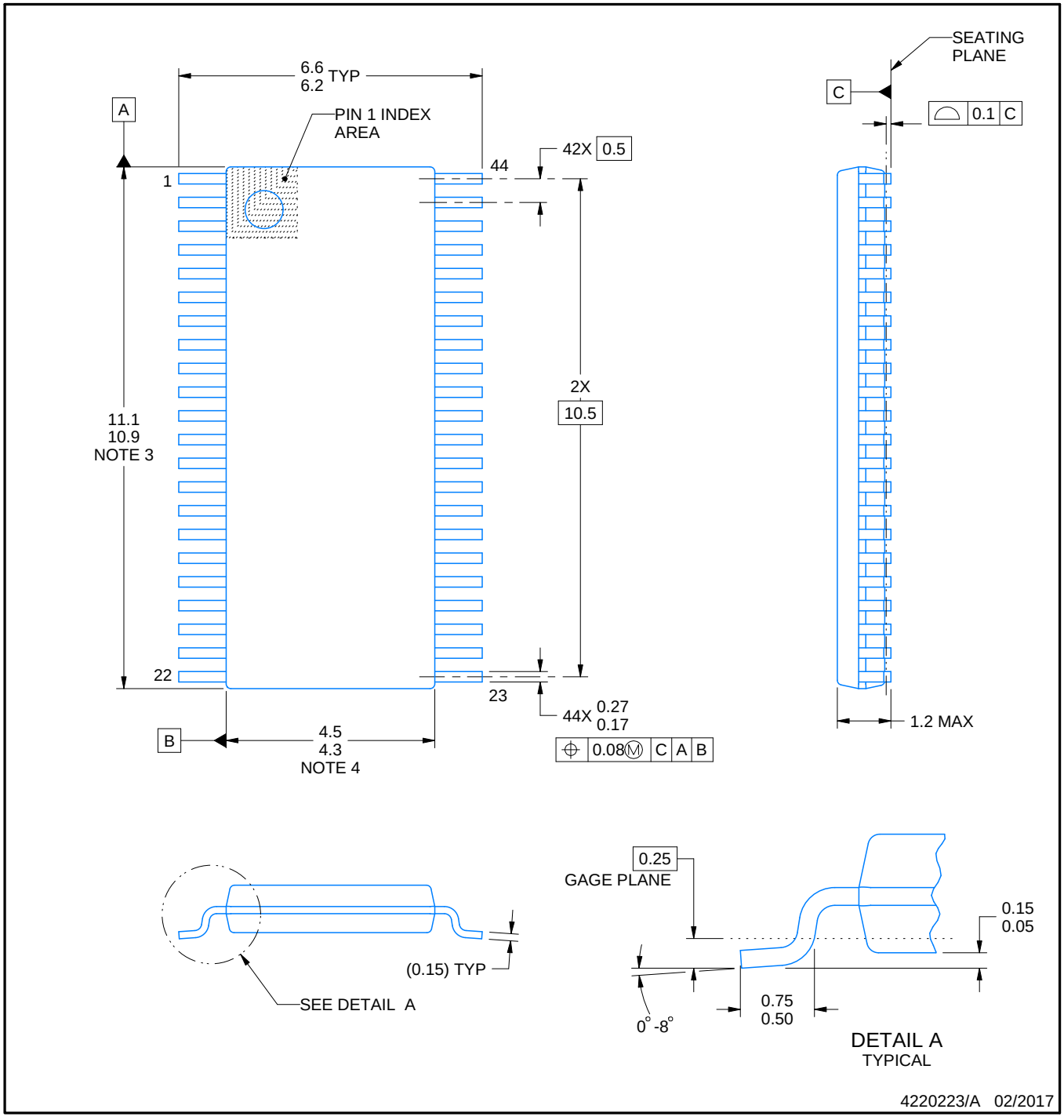
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ20Z655DBTR-R1	TSSOP	DBT	44	2000	367.0	367.0	45.0

PACKAGE OUTLINE

DBT0044A

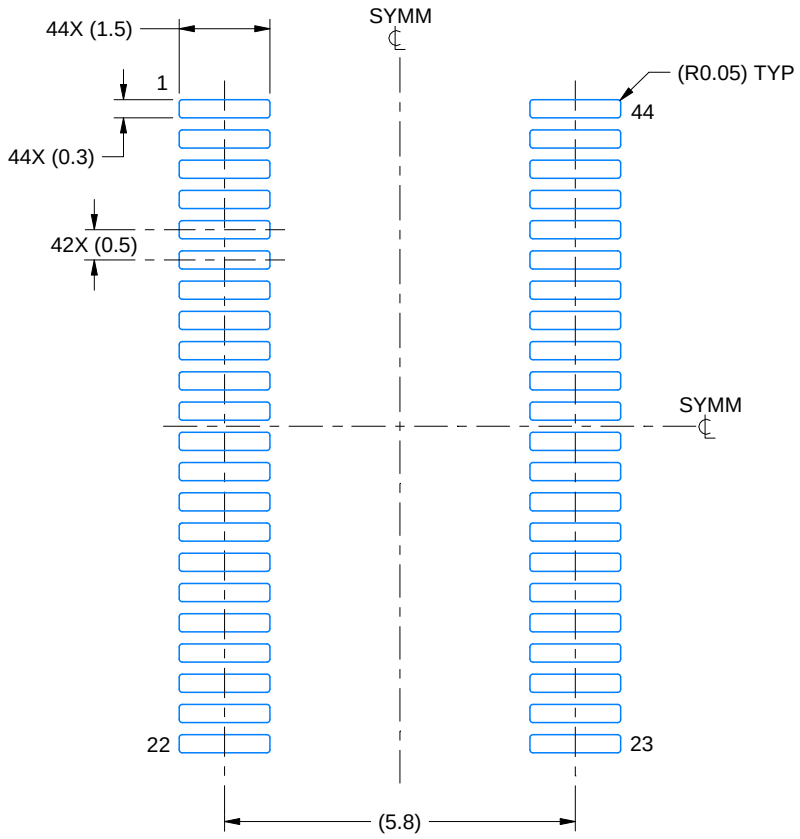
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

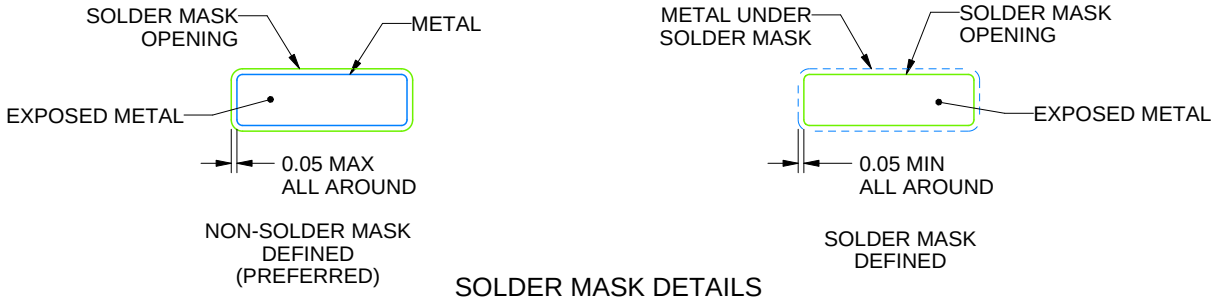


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X

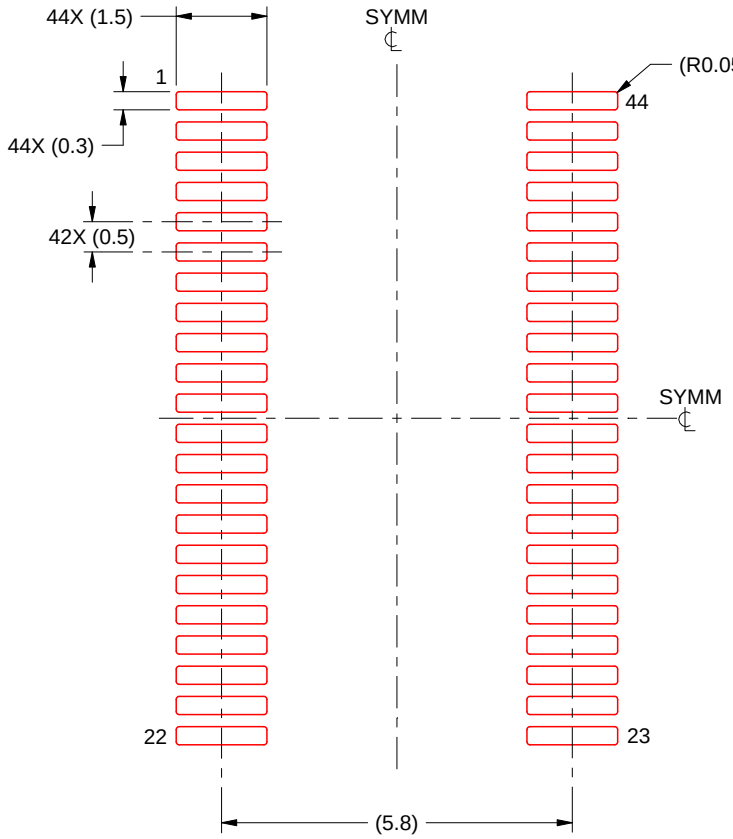


SOLDER MASK DETAILS

4220223/A 02/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

4220223/A 02/2017

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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